

RL78/G13

R01DS0131EJ0200

RENESAS MCU

Rev.2.00

Oct 12, 2012

True Low Power Platform (as low as 66 $\mu\text{A}/\text{MHz}$, and 0.57 μA for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 512 Kbyte Flash, 41 DMIPS at 32 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology

- 1.6 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA , (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.57 μA
- Snooze: 0.70 mA (UART), 1.20 mA (ADC)
- Operating: 66 $\mu\text{A}/\text{MHz}$

16-bit RL78 CPU Core

- Delivers 41 DMIPS at maximum operating frequency of 32 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Main Flash Memory

- Density: 16 KB to 512 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory

- Data Flash with background operation
- Data flash size: 4 KB to 8 KB size options
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 1.8 V to 5.5 V

RAM

- 2 KB to 32 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator

- 32 MHz with +/- 1% accuracy over voltage (1.8 V to 5.5 V) and temperature (-20 °C to 85 °C)
- Pre-configured settings: 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 4 MHz & 1 MHz

Reset and Supply Management

- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 14 setting options (Interrupt and/or reset function)

Data Memory Access (DMA) Controller

- Up to 4 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces

- Up to 8 x I²C master
- Up to 2 x I²C multi-master
- Up to 8 x CSI/SPI (7-, 8-bit)
- Up to 4 x UART (7-, 8-, 9-bit)
- Up to 1 x LIN

Extended-Function Timers

- Multi-function 16-bit timers: Up to 16 channels
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- Interval Timer: 12-bit, 1 channel
- 15 kHz watchdog timer : 1 channel (window function)

Rich Analog

- ADC: Up to 26 channels, 10-bit resolution, 2.1 μs conversion time
- Supports 1.6 V
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)

- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/ frequency detection
- ADC self-test

General Purpose I/O

- 5V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature

- Standard: -40 °C to +85 °C
- Extended: -40 °C to +105 °C

Package Type and Pin Count

From 3mm x 3mm to 14mm x 20mm
 QFP: 44, 48, 52, 64, 80, 100, 128
 QFN: 24, 32, 40, 48
 SSOP: 20, 30
 LGA: 25, 36
 BGA: 64

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G13					
			20 pins	24 pins	25 pins	30 pins	32 pins	36 pins
128 KB	8 KB	12 KB	–	–	–	R5F100AG	R5F100BG	R5F100CG
	–		–	–	R5F101AG	R5F101BG	R5F101CG	
96 KB	8 KB	8 KB	–	–	–	R5F100AF	R5F100BF	R5F100CF
	–		–	–	R5F101AF	R5F101BF	R5F101CF	
64 KB	4 KB	4 KB <i>Note 1</i>	R5F1006E	R5F1007E	R5F1008E	R5F100AE	R5F100BE	R5F100CE
	–		R5F1016E	R5F1017E	R5F1018E	R5F101AE	R5F101BE	R5F101CE
48 KB	4 KB	3 KB	R5F1006D	R5F1007D	R5F1008D	R5F100AD	R5F100BD	R5F100CD
	–		R5F1016D	R5F1017D	R5F1018D	R5F101AD	R5F101BD	R5F101CD
32 KB	4 KB	2 KB	R5F1006C	R5F1007C	R5F1008C	R5F100AC	R5F100BC	R5F100CC
	–		R5F1016C	R5F1017C	R5F1018C	R5F101AC	R5F101BC	R5F101CC
16 KB	4 KB	2 KB	R5F1006A	R5F1007A	R5F1008A	R5F100AA	R5F100BA	R5F100CA
	–		R5F1016A	R5F1017A	R5F1018A	R5F101AA	R5F101BA	R5F101CA

Flash ROM	Data flash	RAM	RL78/G13							
			40 pins	44 pins	48 pins	52 pins	64 pins	80 pins	100 pins	128 pins
512 KB	8 KB	32 KB <i>Note 3</i>	–	R5F100FL	R5F100GL	R5F100JL	R5F100LL	R5F100ML	R5F100PL	R5F100SL
	–		–	R5F101FL	R5F101GL	R5F101JL	R5F101LL	R5F101ML	R5F101PL	R5F101SL
384 KB	8 KB	24 KB	–	R5F100FK	R5F100GK	R5F100JK	R5F100LK	R5F100MK	R5F100PK	R5F100SK
	–		–	R5F101FK	R5F101GK	R5F101JK	R5F101LK	R5F101MK	R5F101PK	R5F101SK
256 KB	8 KB	20 KB <i>Note 2</i>	–	R5F100FJ	R5F100GJ	R5F100JJ	R5F100LJ	R5F100MJ	R5F100PJ	R5F100SJ
	–		–	R5F101FJ	R5F101GJ	R5F101JJ	R5F101LJ	R5F101MJ	R5F101PJ	R5F101SJ
192 KB	8 KB	16 KB	R5F100EH	R5F100FH	R5F100GH	R5F100JH	R5F100LH	R5F100MH	R5F100PH	R5F100SH
	–		R5F101EH	R5F101FH	R5F101GH	R5F101JH	R5F101LH	R5F101MH	R5F101PH	R5F101SH
128 KB	8 KB	12 KB	R5F100EG	R5F100FG	R5F100GG	R5F100JG	R5F100LG	R5F100MG	R5F100PG	–
	–		R5F101EG	R5F101FG	R5F101GG	R5F101JG	R5F101LG	R5F101MG	R5F101PG	–
96 KB	8 KB	8 KB	R5F100EF	R5F100FF	R5F100GF	R5F100JF	R5F100LF	R5F100MF	R5F100PF	–
	–		R5F101EF	R5F101FF	R5F101GF	R5F101JF	R5F101LF	R5F101MF	R5F101PF	–
64 KB	4 KB	4 KB <i>Note 1</i>	R5F100EE	R5F100FE	R5F100GE	R5F100JE	R5F100LE	–	–	–
	–		R5F101EE	R5F101FE	R5F101GE	R5F101JE	R5F101LE	–	–	–
48 KB	4 KB	3 KB	R5F100ED	R5F100FD	R5F100GD	R5F100JD	R5F100LD	–	–	–
	–		R5F101ED	R5F101FD	R5F101GD	R5F101JD	R5F101LD	–	–	–
32 KB	4 KB	2 KB	R5F100EC	R5F100FC	R5F100GC	R5F100JC	R5F100LC	–	–	–
	–		R5F101EC	R5F101FC	R5F101GC	R5F101JC	R5F101LC	–	–	–
16 KB	4 KB	2 KB	R5F100EA	R5F100FA	R5F100GA	–	–	–	–	–
	–		R5F101EA	R5F101FA	R5F101GA	–	–	–	–	–

- Notes**
1. This is about 3 KB when the self-programming function and data flash function are used.
 2. This is about 19 KB when the self-programming function and data flash function are used.
 3. This is about 31 KB when the self-programming function and data flash function are used.

1.2 Ordering Information

- Flash memory version (lead-free product)

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Pin count	Package	Data flash	Part Number
20 pins	20-pin plastic SSOP (7.62 mm (300))	Mounted	R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
		Not mounted	R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP
24 pins	24-pin plastic WQFN (fine pitch) (4 × 4)	Mounted	R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
		Not mounted	R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA
25 pins	25-pin plastic FLGA (3 × 3)	Mounted	R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA R5F1008ADLA, R5F1008CDLA, R5F1008DDLA, R5F1008EDLA
		Not mounted	R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA R5F1018ADLA, R5F1018CDLA, R5F1018DDLA, R5F1018EDLA
30 pins	30-pin plastic SSOP (7.62 mm (300))	Mounted	R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
		Not mounted	R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP
32 pins	32-pin plastic WQFN (fine pitch)(5 × 5)	Mounted	R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
		Not mounted	R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA
36 pins	36-pin plastic FLGA (4 × 4)	Mounted	R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA R5F100CADLA, R5F100CCDLA, R5F100CDDL, R5F100CEDLA, R5F100CFDLA, R5F100CGDLA
		Not mounted	R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA R5F101CADLA, R5F101CCDLA, R5F101CDDL, R5F101CEDLA, R5F101CFDLA, R5F101CGDLA

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Pin count	Package	Data flash	Part Number
40 pins	40-pin plastic WQFN (fine pitch)(6 × 6)	Mounted	R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA
		Not mounted	R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA
44 pins	44-pin plastic LQFP (10 × 10)	Mounted	R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP, R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP, R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
		Not mounted	R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP, R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP, R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	Mounted	R5F100GAAFB, R5F100GCAFB, R5F100GDAFB, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB, R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB R5F100GADFB, R5F100GCDFB, R5F100GDDB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB, R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
		Not mounted	R5F101GAAFB, R5F101GCAFB, R5F101GDAFB, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB, R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB R5F101GADFB, R5F101GCDFB, R5F101GDDB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB, R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB
	48-pin plastic WQFN (7 × 7)	Mounted	R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA, R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA, R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
		Not mounted	R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA, R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA, R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA

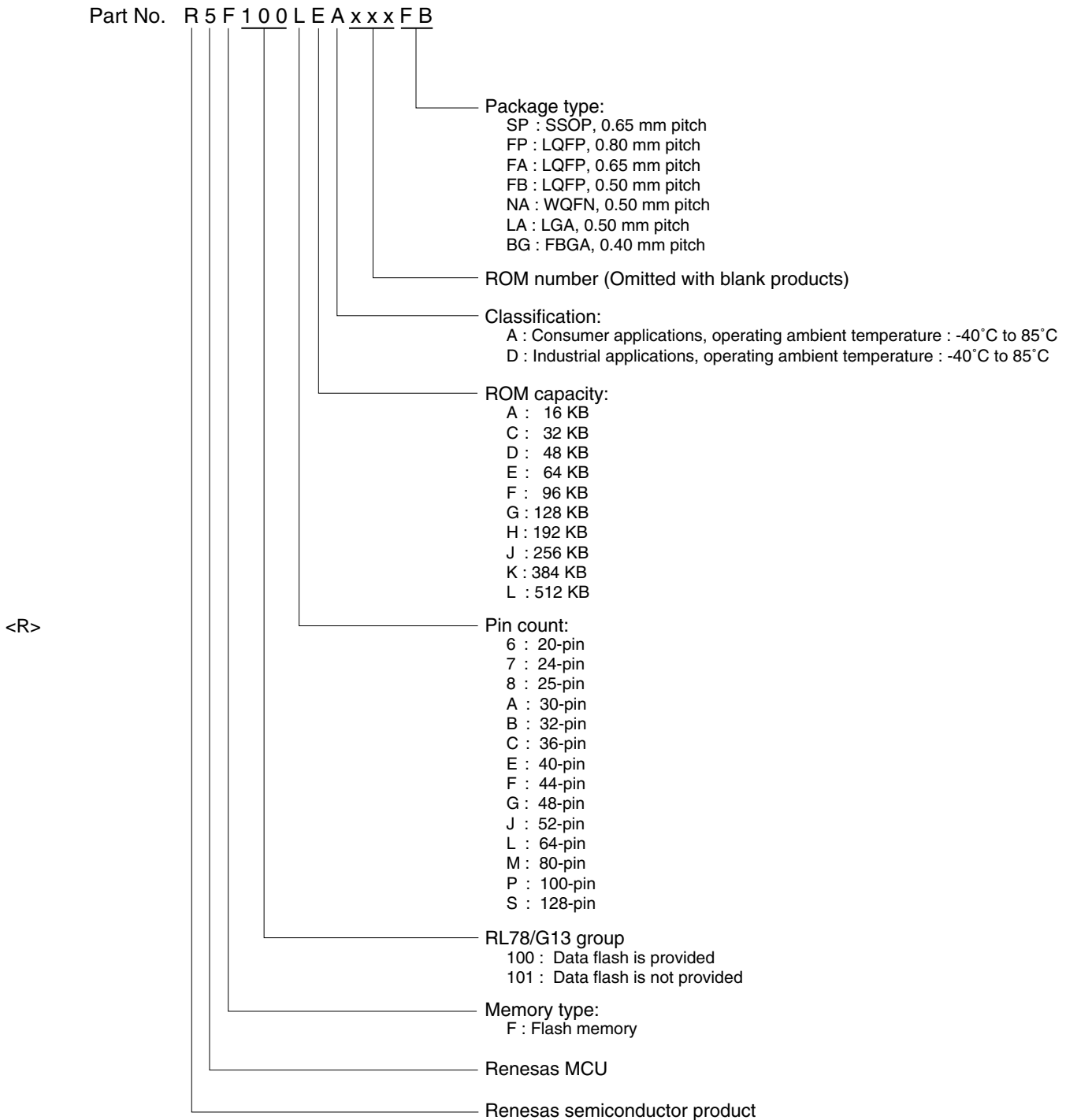
(3/4)

Pin count	Package	Data flash	Part Number	
52 pins	52-pin plastic LQFP (10 × 10)	Mounted	R5F100JCAFA, R5F100JDAFA, R5F100JEAF A, R5F100JFAFA, R5F100JGAF A, R5F100JHAF A, R5F100JJAF A, R5F100JKAF A, R5F100JLAF A R5F100JCDF A, R5F100JDDF A, R5F100JEDF A, R5F100JFDF A, R5F100JGDF A, R5F100JHDF A, R5F100JJDF A, R5F100JKDF A, R5F100JLDF A	
		Not mounted	R5F101JCAFA, R5F101JDAFA, R5F101JEAF A, R5F101JFAFA, R5F101JGAF A, R5F101JHAF A, R5F101JJAF A, R5F101JKAF A, R5F101JLAF A R5F101JCDF A, R5F101JDDF A, R5F101JEDF A, R5F101JFDF A, R5F101JGDF A, R5F101JHDF A, R5F101JJDF A, R5F101JKDF A, R5F101JLDF A	
64 pins	64-pin plastic LQFP (12 × 12)	Mounted	R5F100LCAFA, R5F100LDAFA, R5F100LEAF A, R5F100LFAFA, R5F100LGAF A, R5F100LHAF A, R5F100LJAF A, R5F100LKAF A, R5F100LLAF A R5F100LCDF A, R5F100LDDF A, R5F100LEDF A, R5F100LFDF A, R5F100LGDF A, R5F100LHDF A, R5F100LJDF A, R5F100LKDF A, R5F100LLDF A	
		Not mounted	R5F101LCAFA, R5F101LDAFA, R5F101LEAF A, R5F101LFAFA, R5F101LGAF A, R5F101LHAF A, R5F101LJAF A, R5F101LKAF A, R5F101LLAF A R5F101LCDF A, R5F101LDDF A, R5F101LEDF A, R5F101LFDF A, R5F101LGDF A, R5F101LHDF A, R5F101LJDF A, R5F101LKDF A, R5F101LLDF A	
	64-pin plastic LQFP (fine pitch) (10 × 10)	Mounted	R5F100LCAFB, R5F100LDAFB, R5F100LEAF B, R5F100LFAFB, R5F100LGAF B, R5F100LHAF B, R5F100LJAF B, R5F100LKAF B, R5F100LLAF B R5F100LCDF B, R5F100LDDF B, R5F100LEDF B, R5F100LFDF B, R5F100LGDF B, R5F100LHDF B, R5F100LJDF B, R5F100LKDF B, R5F100LLDF B	
		Not mounted	R5F101LCAFB, R5F101LDAFB, R5F101LEAF B, R5F101LFAFB, R5F101LGAF B, R5F101LHAF B, R5F101LJAF B, R5F101LKAF B, R5F101LLAF B R5F101LCDF B, R5F101LDDF B, R5F101LEDF B, R5F101LFDF B, R5F101LGDF B, R5F101LHDF B, R5F101LJDF B, R5F101LKDF B, R5F101LLDF B	
	64-pin plastic FBGA (4 × 4)	Mounted	Mounted	R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG R5F100LCDBG, R5F100LDDBG, R5F100LEDBG, R5F100LFDBG, R5F100LGDBG, R5F100LHDBG, R5F100LJDBG
			Not mounted	R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG R5F101LCDBG, R5F101LDDBG, R5F101LEDBG, R5F101LFDBG, R5F101LGDBG, R5F101LHDBG, R5F101LJDBG

(4/4)

Pin count	Package	Data flash	Part Number
80 pins	80-pin plastic LQFP (14 × 14)	Mounted	R5F100MFAFA, R5F100MGAGA, R5F100MHAGA, R5F100MJAGA, R5F100MKAGA, R5F100MLAGA R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
		Not mounted	R5F101MFAFA, R5F101MGAGA, R5F101MHAGA, R5F101MJAGA, R5F101MKAGA, R5F101MLAGA R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA
	80-pin plastic LQFP (fine pitch) (12 × 12)	Mounted	R5F100MFAFB, R5F100MGAFB, R5F100MHA FB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB R5F100MFD FB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
		Not mounted	R5F101MFAFB, R5F101MGAFB, R5F101MHA FB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB R5F101MFD FB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB
100 pins	100-pin plastic LQFP (fine pitch) (14 × 14)	Mounted	R5F100PFAFB, R5F100PGA FB, R5F100PHA FB, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB R5F100PFDFB, R5F100PGDFB, R5F100PHDFB, R5F100PJDFB, R5F100PKDFB, R5F100PLDFB
		Not mounted	R5F101PFAFB, R5F101PGA FB, R5F101PHA FB, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB R5F101PFDFB, R5F101PGDFB, R5F101PHDFB, R5F101PJDFB, R5F101PKDFB, R5F101PLDFB
	100-pin plastic LQFP (14 × 20)	Mounted	R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFA, R5F100PLAFA R5F100PFDFB, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA
		Not mounted	R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFA, R5F101PLAFA R5F101PFDFB, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA
128 pins	128-pin plastic LQFP (fine pitch) (14 × 20)	Mounted	R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
		Not mounted	R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

Figure 1-1. Part Number, Memory Size, and Package of RL78/G13

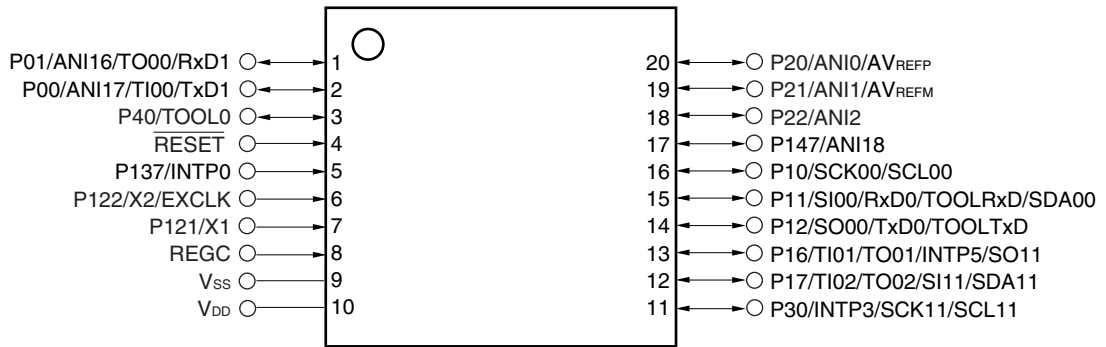


Remark For details about extended-temperature products (operating ambient temperature: -40°C to 105°C), contact a Renesas Electronics Corporation or an authorized Renesas Electronics Corporation distributor.

1.3 Pin Configuration (Top View)

1.3.1 20-pin products

- 20-pin plastic SSOP (7.62 mm (300))

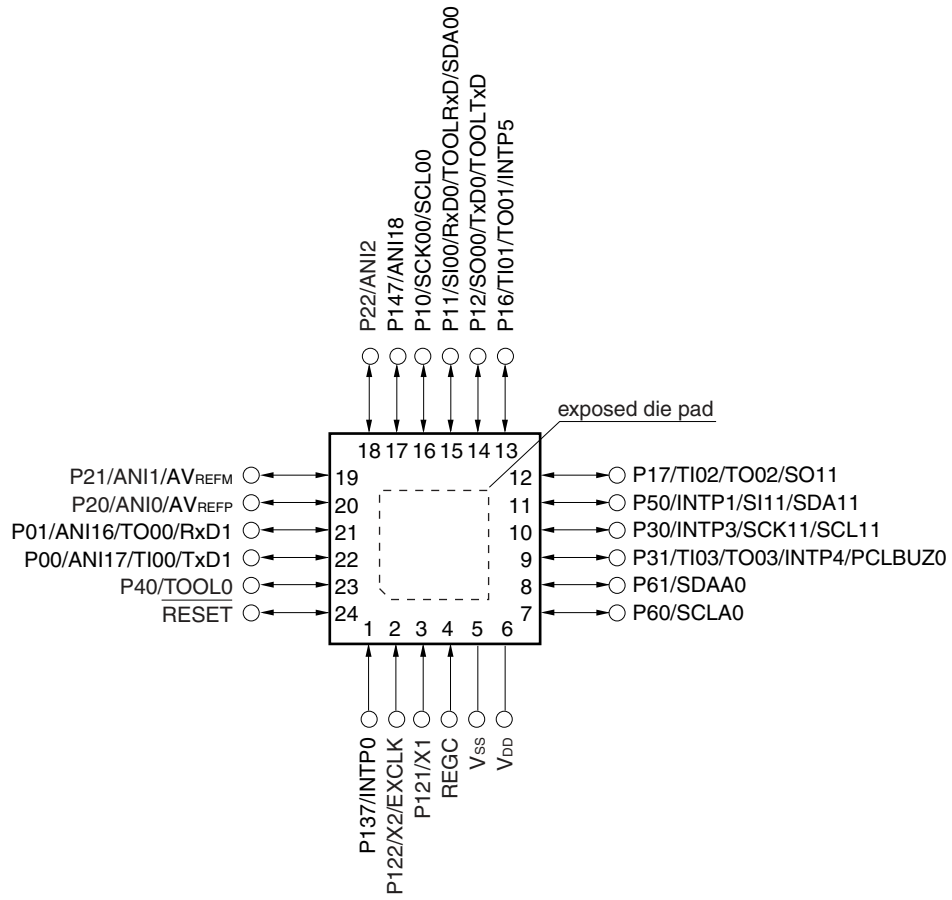


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark For pin identification, see 1.4 Pin Identification.

1.3.2 24-pin products

- 24-pin plastic WQFN (fine pitch) (4 × 4)

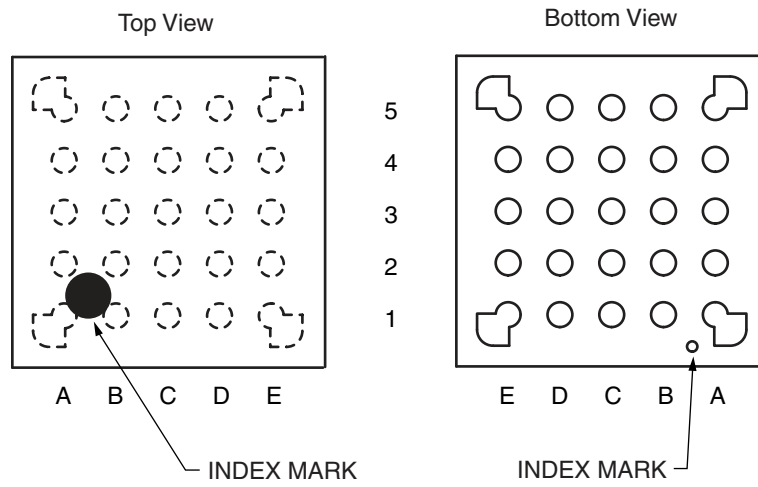


Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark For pin identification, see 1.4 Pin Identification.

1.3.3 25-pin products

- 25-pin plastic FLGA (3 × 3)



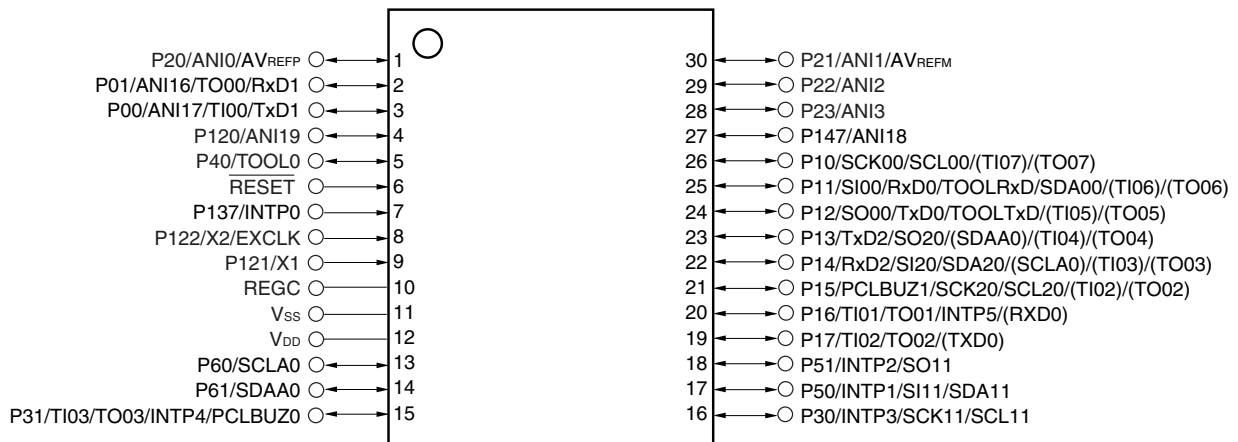
	A	B	C	D	E	
5	P40/TOOL0	RESET	P01/ANI16/ TO00/RxD1	P22/ANI2	P147/ANI18	5
4	P122/X2/ EXCLK	P137/INTP0	P00/ANI17/ TI00/TxD1	P21/ANI1/ AVREFM	P10/SCK00/ SCL00	4
3	P121/X1	V _{DD}	P20/ANI0/ AVREFP	P12/SO00/ TxD0/ TOOLTxD	P11/SI00/ RxD0/ TOOLRxD/ SDA00	3
2	REGC	V _{SS}	P30/INTP3/ SCK11/SCL11	P17/TI02/ TO02/SO11	P50/INTP1/ SI11/SDA11	2
1	P60/SCLA0	P61/SDAA0	P31/TI03/ TO03/INTP4/ PCLBUZ0	P16/TI01/ TO01/INTP5	P130	1
	A	B	C	D	E	

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark For pin identification, see 1.4 Pin Identification.

1.3.4 30-pin products

- 30-pin plastic SSOP (7.62 mm (300))



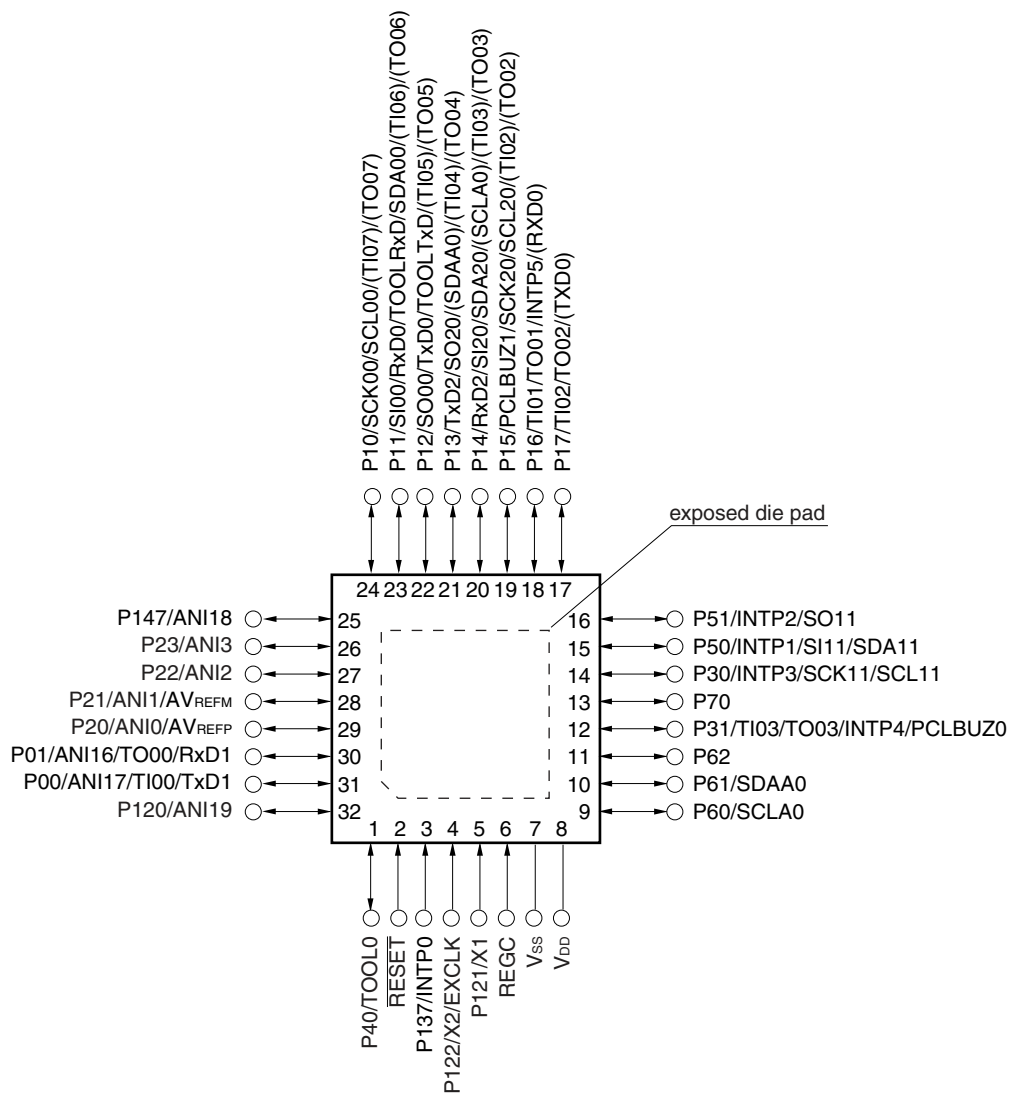
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.5 32-pin products

- 32-pin plastic WQFN (5 × 5)



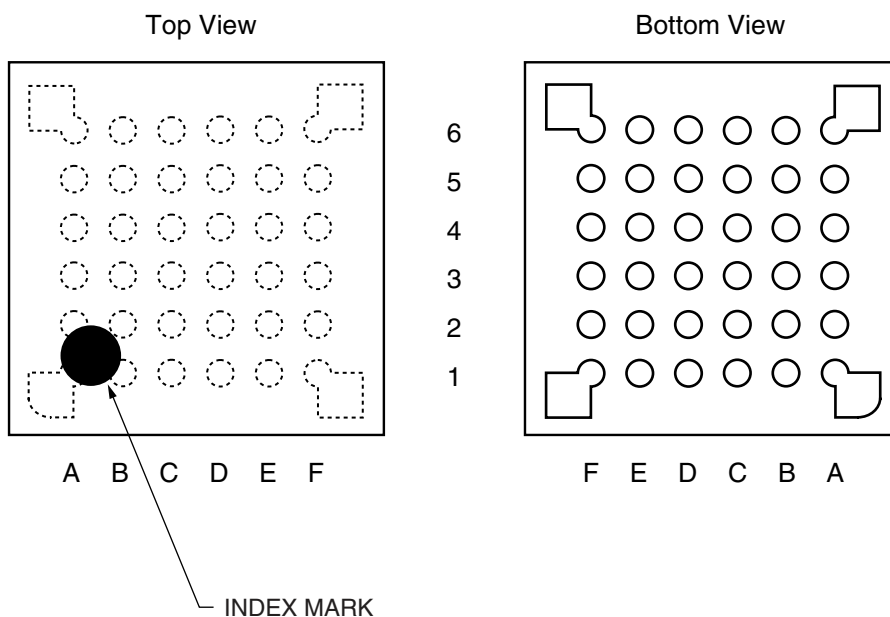
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.6 36-pin products

- 36-pin plastic FLGA (4 × 4)



	A	B	C	D	E	F	
6	P60/SCLA0	V _{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62	P61/SDAA0	V _{SS}	REGC	RESET	P120/ANI19	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/(SCLA0) /(TI03)/(TO03)	P31/TI03/TO03/ INTP4/ PCLBUZ0	P00/TI00/TxD1	P01/TO00/RxD1	4
3	P50/INTP1/ SI11/SDA11	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2	P20/ANI0/ AV _{REFP}	P21/ANI1/ AV _{REFM}	3
2	P30/INTP3/ SCK11/SCL11	P16/TI01/TO01/ INTP5/(RxD0)	P12/SO00/ TxD0/TOOLTxD /(TI05)/(TO05)	P11/SI00/RxD0/ TOOLRxD/ SDA00/(TI06)/ (TO06)	P24/ANI4	P23/ANI3	2
1	P51/INTP2/ SO11	P17/TI02/TO02/ (TxD0)	P13/TxD2/ SO20/(SDAA0)/ (TI04)/(TO04)	P10/SCK00/ SCL00/(TI07)/ (TO07)	P147/ANI18	P25/ANI5	1
	A	B	C	D	E	F	

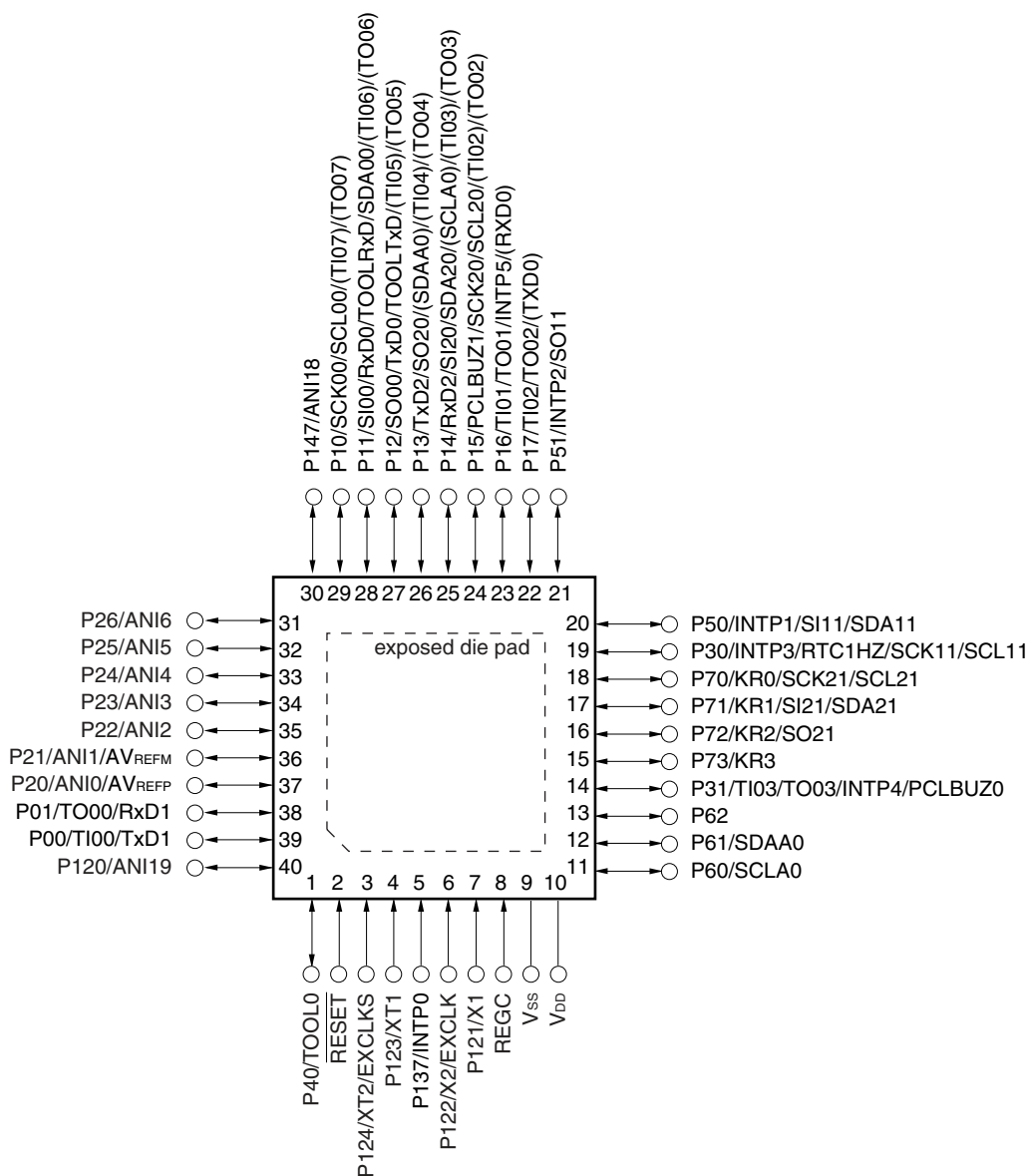
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.7 40-pin products

- 40-pin plastic WQFN (6 × 6)



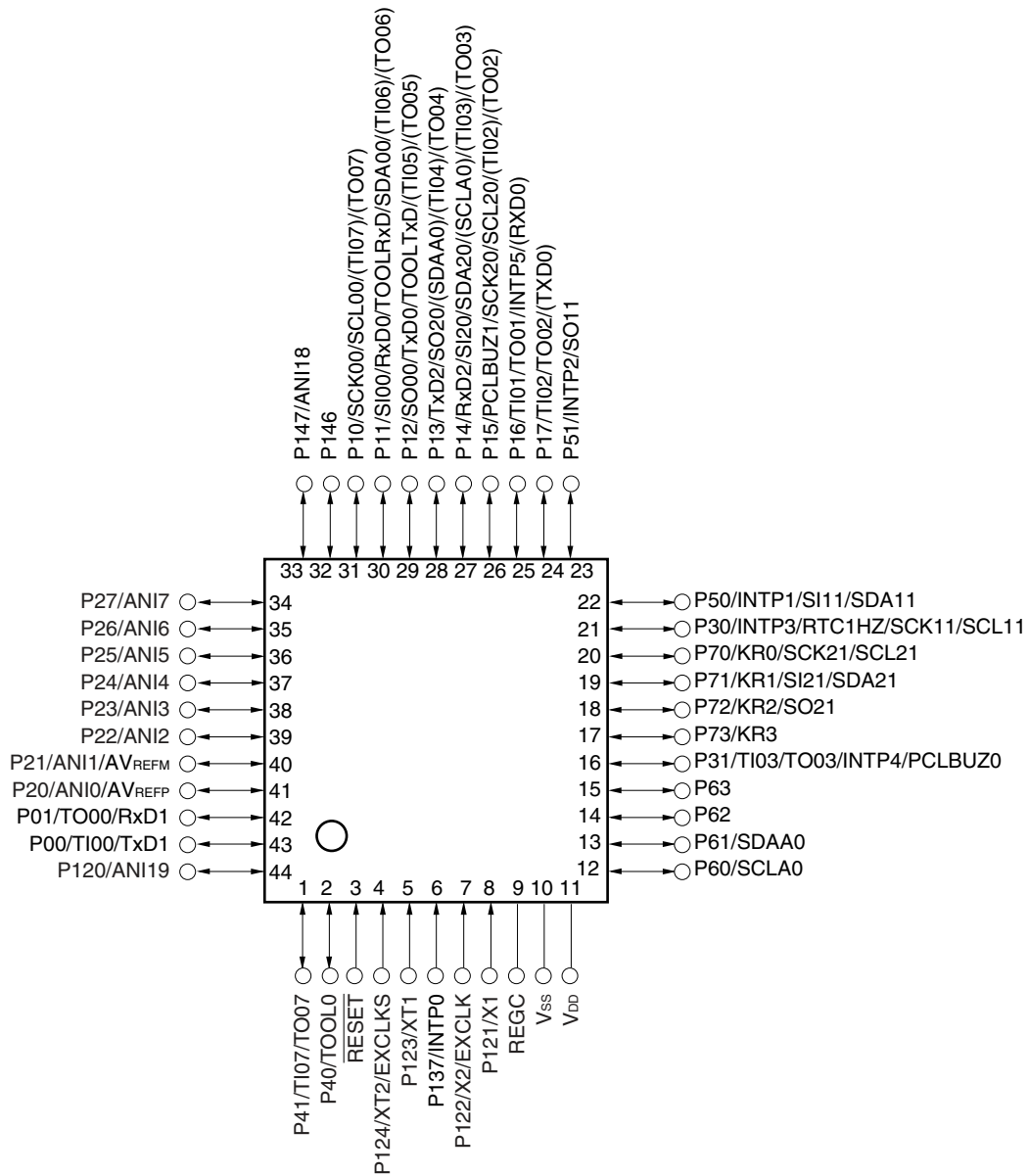
Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.8 44-pin products

- 44-pin plastic LQFP (10 × 10)



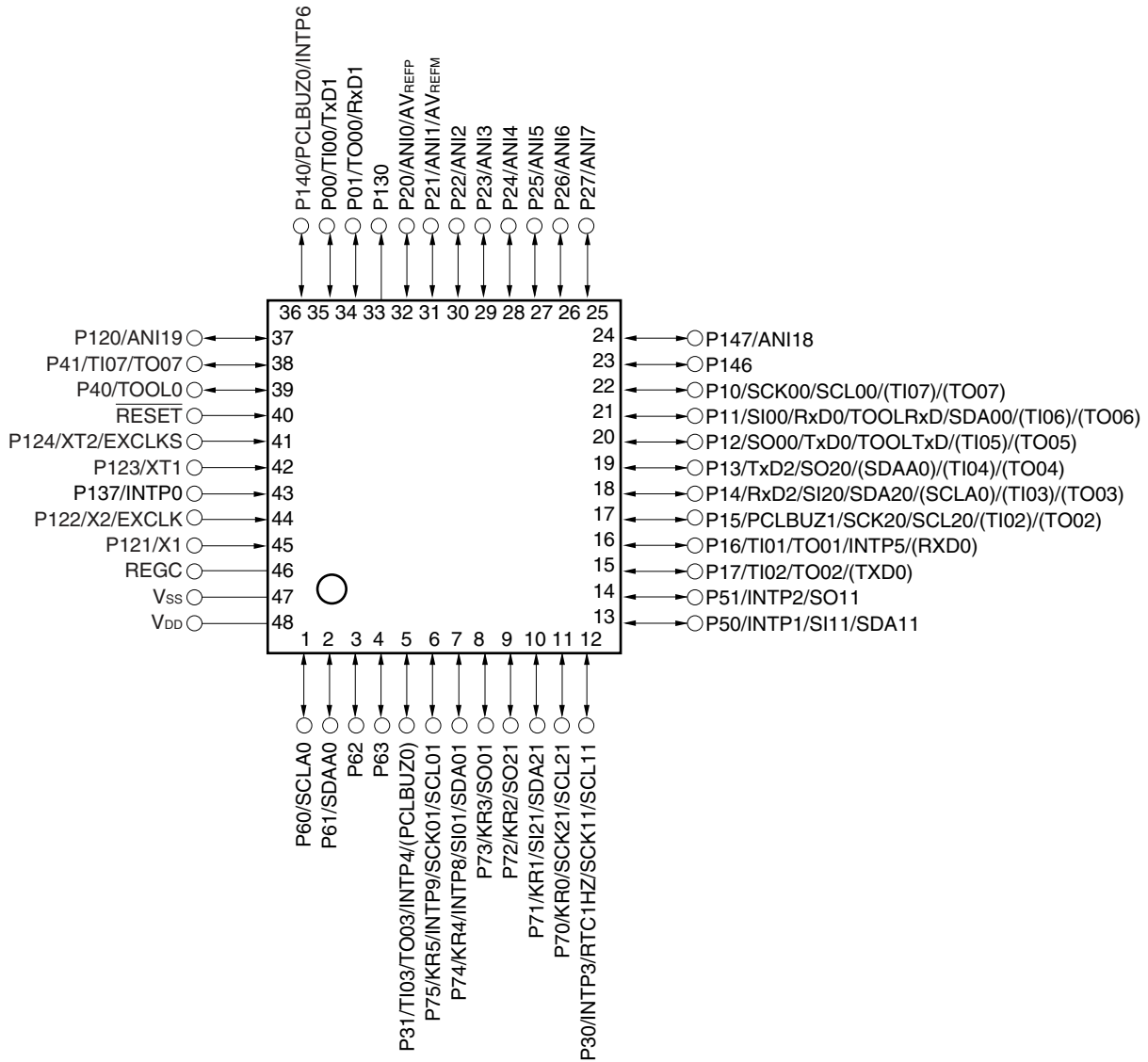
Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.9 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)

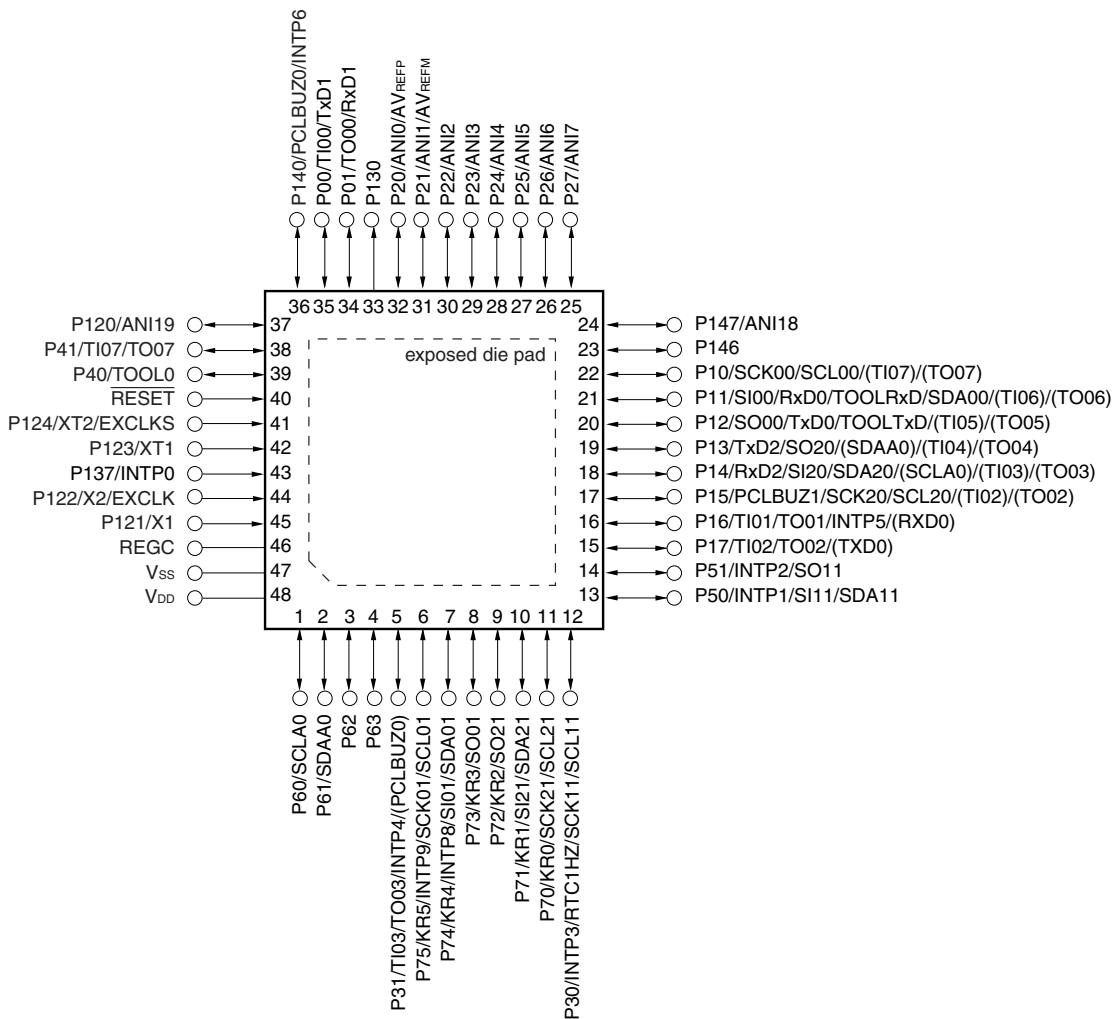


Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μ F).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 48-pin plastic WQFN (7 × 7)



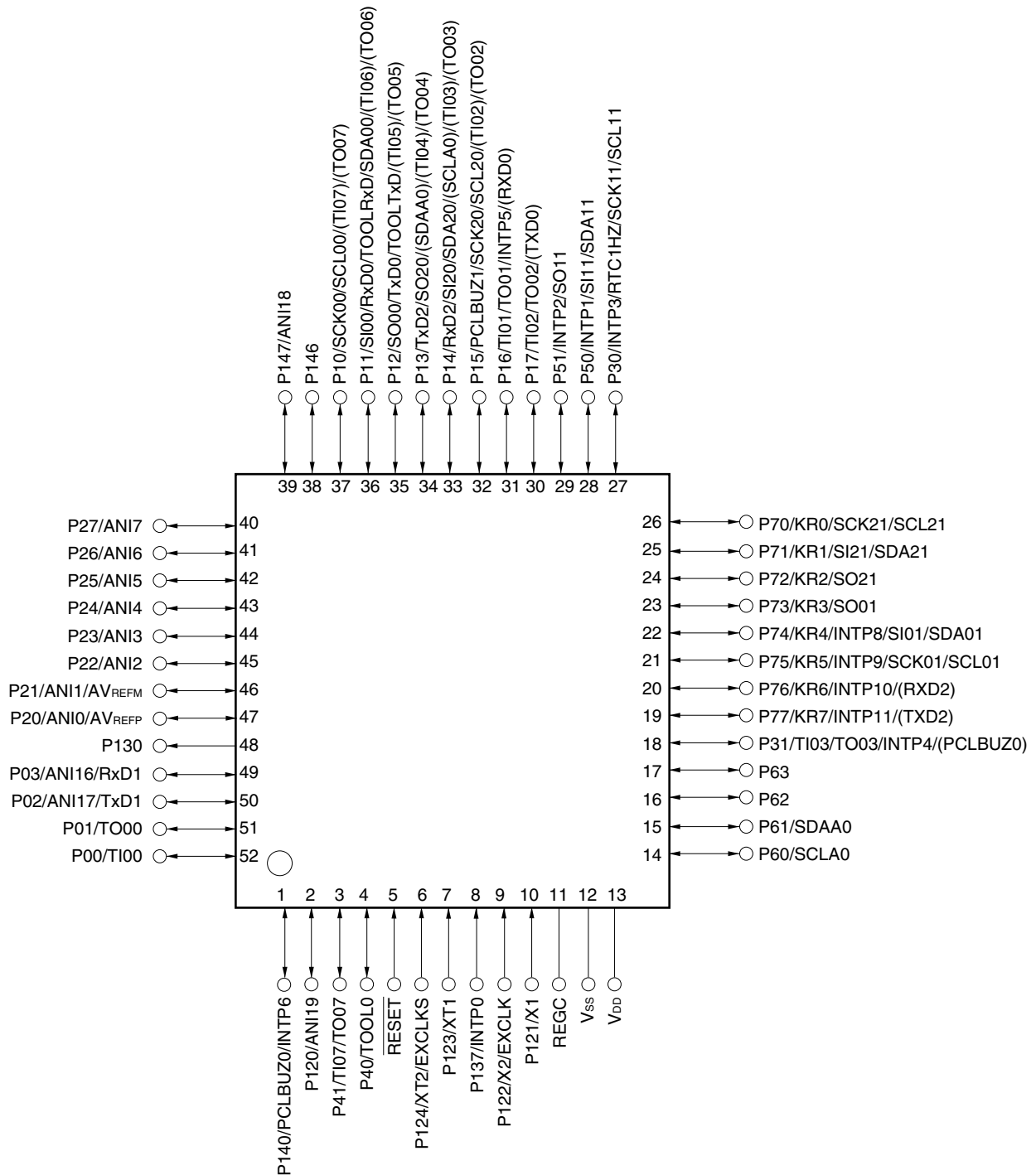
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.10 52-pin products

- 52-pin plastic LQFP (10 × 10)



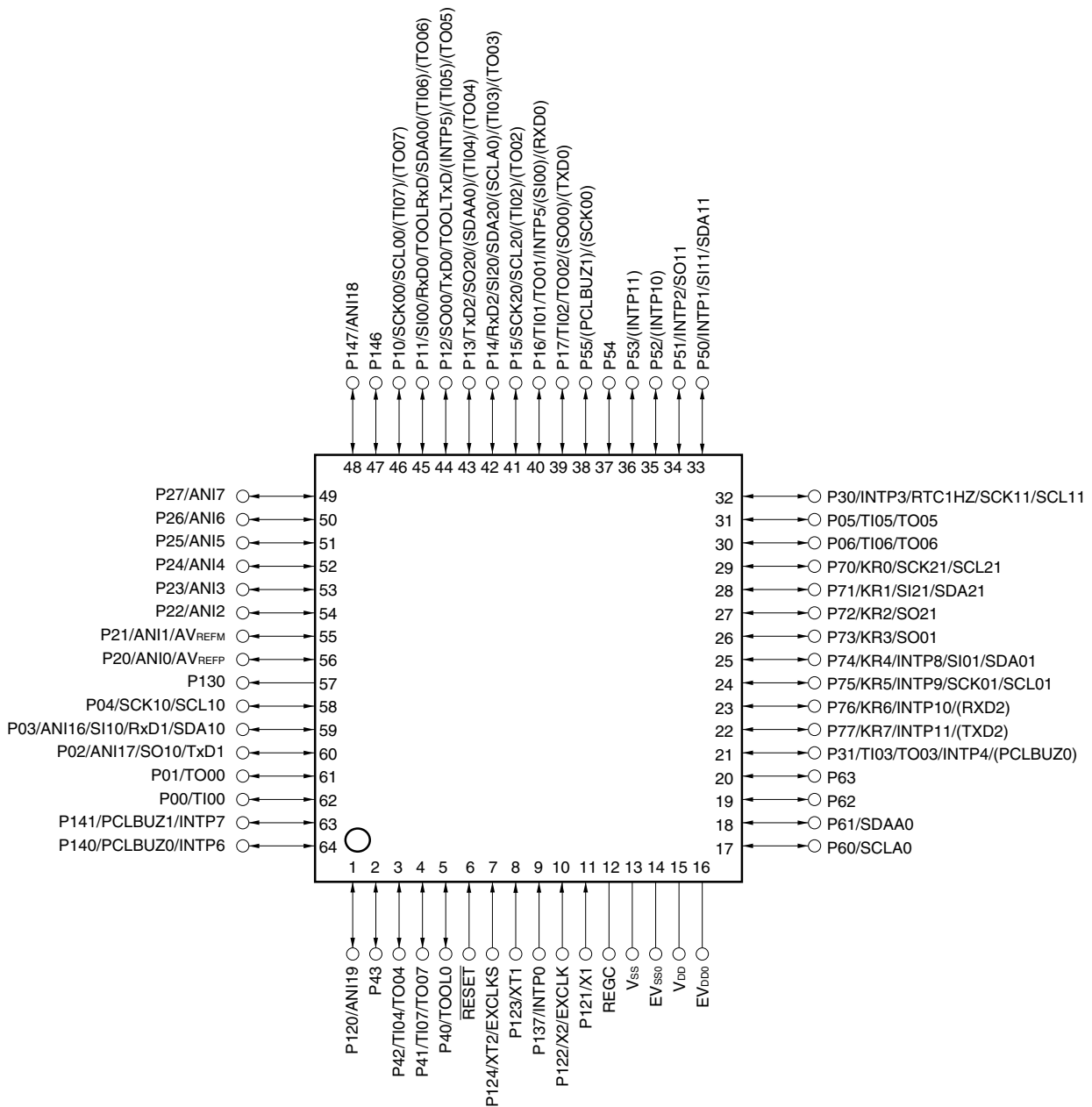
Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see 1.4 Pin Identification.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.11 64-pin products

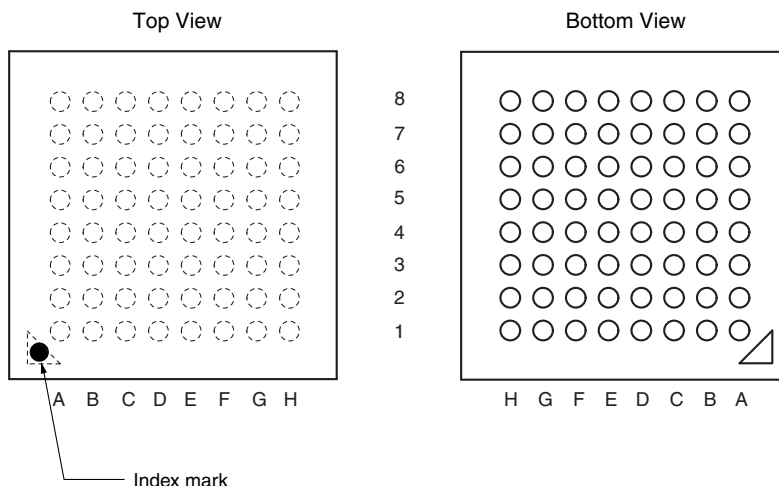
- 64-pin plastic LQFP (12 × 12)
- 64-pin plastic LQFP (fine pitch) (10 × 10)



- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 64-pin plastic FBGA (4 × 4)



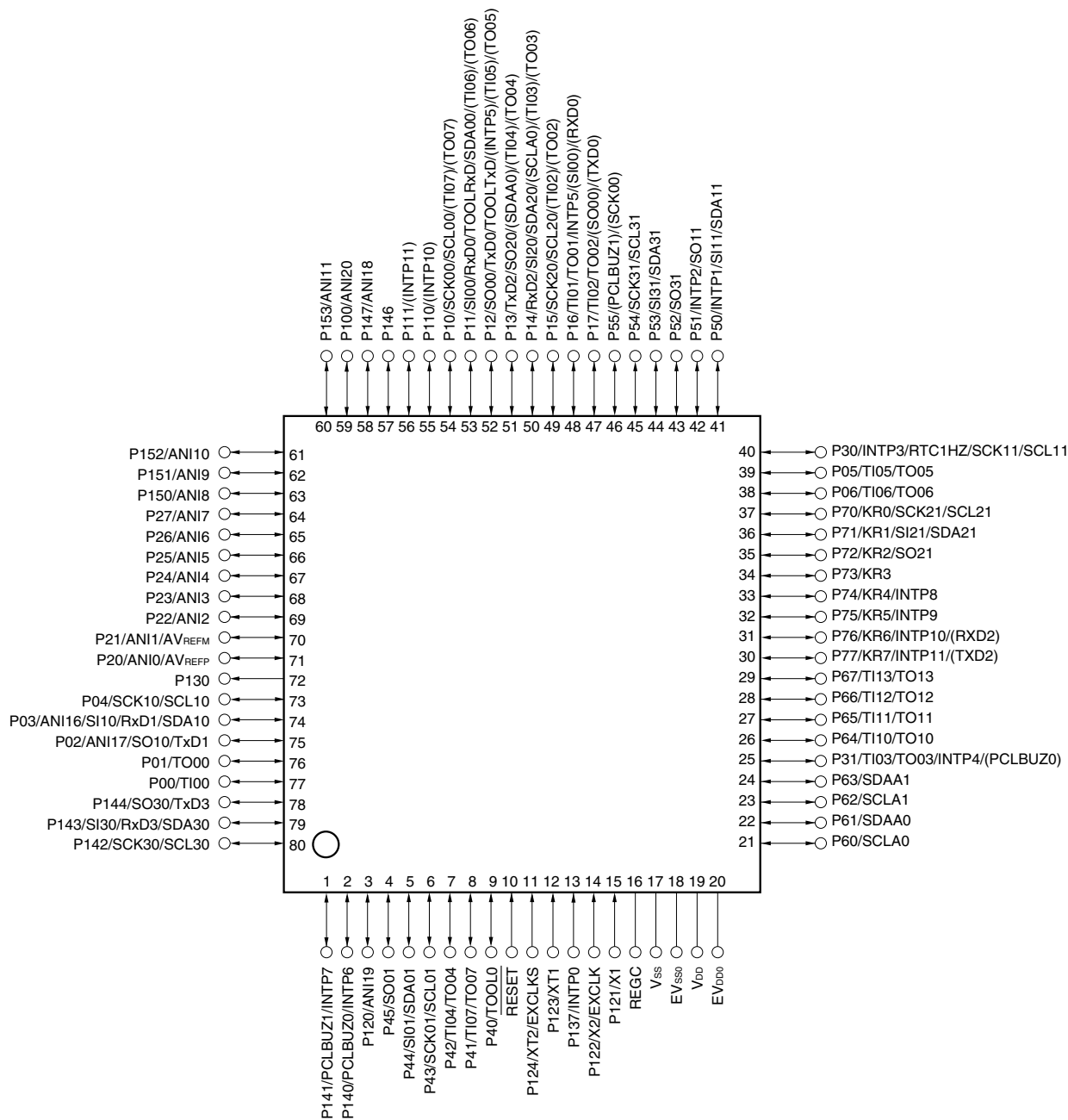
Pin No.	Name	Pin No.	Name	Pin No.	Name	Pin No.	Name
A1	P05/TI05/TO05	C1	P51/INTP2/SO11	E1	P13/TxD2/SO20/ (SDAA0)/(TI04)/(TO04)	G1	P146
A2	P30/INTP3/RTC1HZ /SCK11/SCL11	C2	P71/KR1/SI21/SDA21	E2	P14/RxD2/SI20/SDA20 /(SCLA0)/(TI03)/(TO03)	G2	P25/ANI5
A3	P70/KR0/SCK21 /SCL21	C3	P74/KR4/INTP8/SI01 /SDA01	E3	P15/SCK20/SCL20/ (TI02)/(TO02)	G3	P24/ANI4
A4	P75/KR5/INTP9 /SCK01/SCL01	C4	P52/(INTP10)	E4	P16/TI01/TO01/INTP5 /(SI00)/(RxD0)	G4	P22/ANI2
A5	P77/KR7/INTP11/ (TxD2)	C5	P53/(INTP11)	E5	P03/ANI16/SI10/RxD1 /SDA10	G5	P130
A6	P61/SDAA0	C6	P63	E6	P41/TI07/TO07	G6	P02/ANI17/SO10/TxD1
A7	P60/SCLA0	C7	V _{SS}	E7	RESET	G7	P00/TI00
A8	EV _{DD0}	C8	P121/X1	E8	P137/INTP0	G8	P124/XT2/EXCLKS
B1	P50/INTP1/SI11 /SDA11	D1	P55/(PCLBUZ1)/ (SCK00)	F1	P10/SCK00/SCL00/ (TI07)/(TO07)	H1	P147/ANI18
B2	P72/KR2/SO21	D2	P06/TI06/TO06	F2	P11/SI00/RxD0 /TOOLRxD/SDA00/ (TI06)/(TO06)	H2	P27/ANI7
B3	P73/KR3/SO01	D3	P17/TI02/TO02/ (SO00)/(TxD0)	F3	P12/SO00/TxD0 /TOOLTxD/(INTP5)/ (TI05)/(TO05)	H3	P26/ANI6
B4	P76/KR6/INTP10/ (RxD2)	D4	P54	F4	P21/ANI1/AV _{REFM}	H4	P23/ANI3
B5	P31/TI03/TO03 /INTP4/(PCLBUZ0)	D5	P42/TI04/TO04	F5	P04/SCK10/SCL10	H5	P20/ANI0/AV _{REFP}
B6	P62	D6	P40/TOOL0	F6	P43	H6	P141/PCLBUZ1/INTP7
B7	V _{DD}	D7	REGC	F7	P01/TO00	H7	P140/PCLBUZ0/INTP6
B8	EV _{SS0}	D8	P122/X2/EXCLK	F8	P123/XT1	H8	P120/ANI19

- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.12 80-pin products

- 80-pin plastic LQFP (14 × 14)
- 80-pin plastic LQFP (fine pitch) (12 × 12)

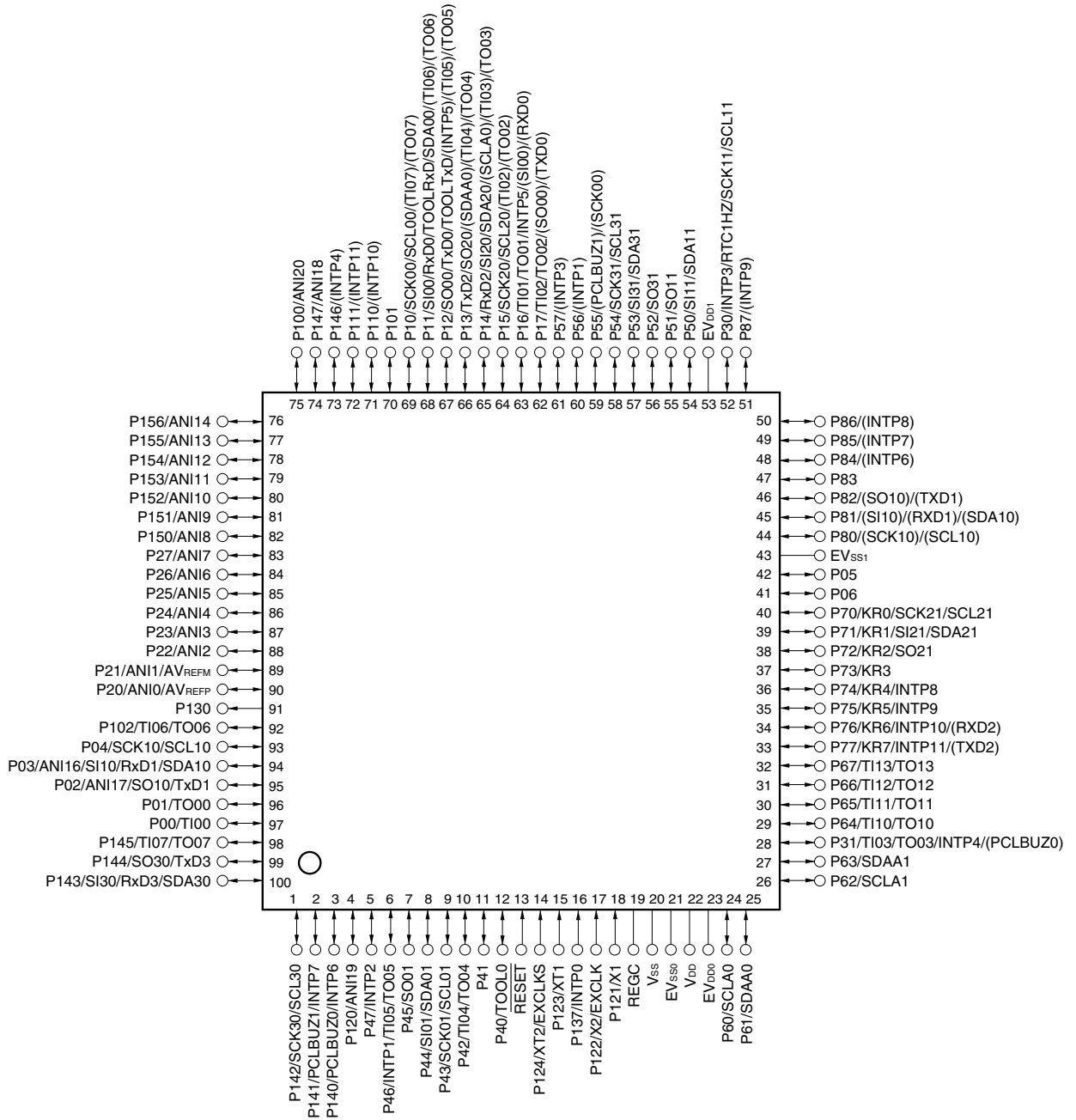


- Cautions**
1. Make EV_{SS0} pin the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.13 100-pin products

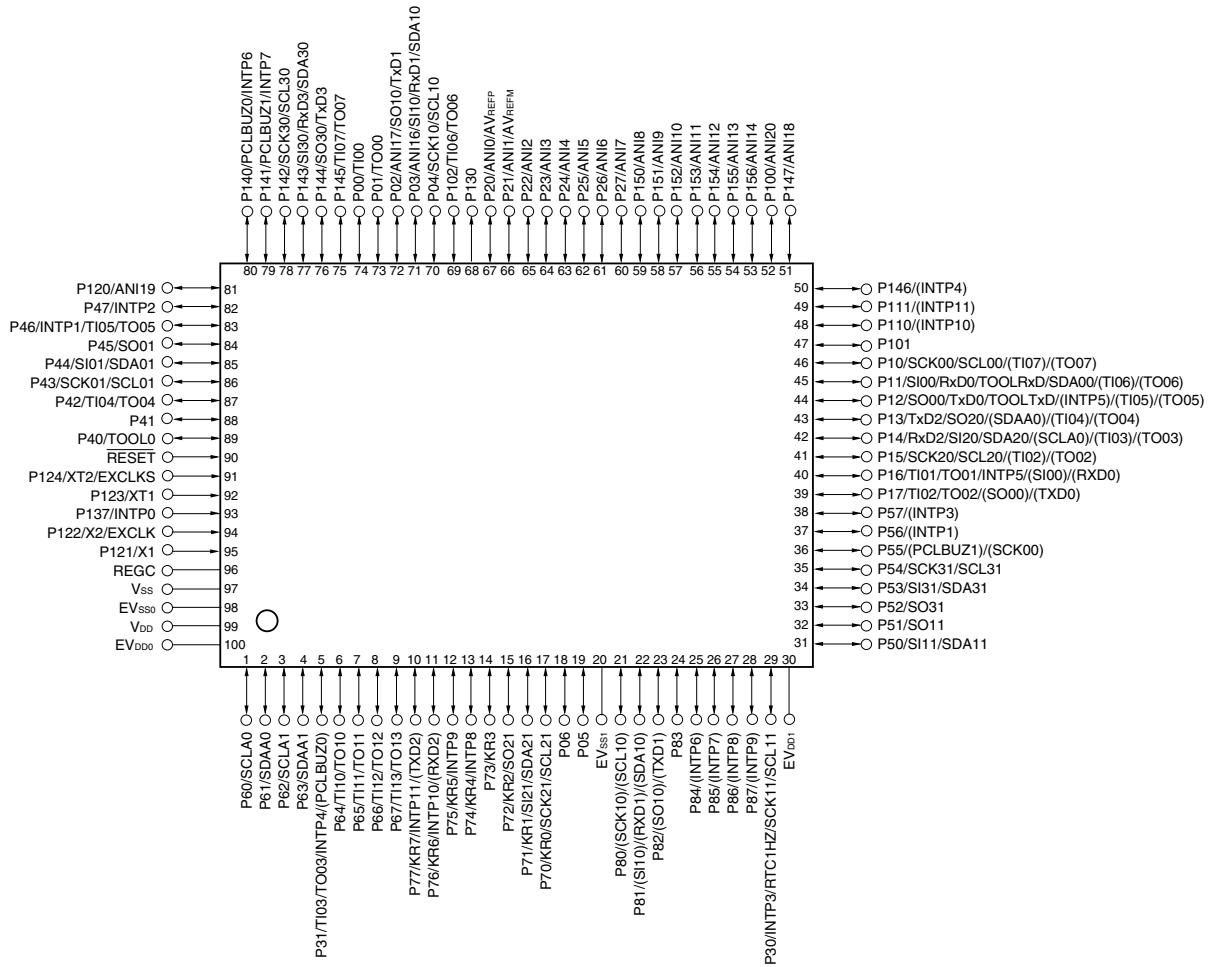
- 100-pin plastic LQFP (fine pitch) (14 × 14)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

- 100-pin plastic LQFP (14 × 20)

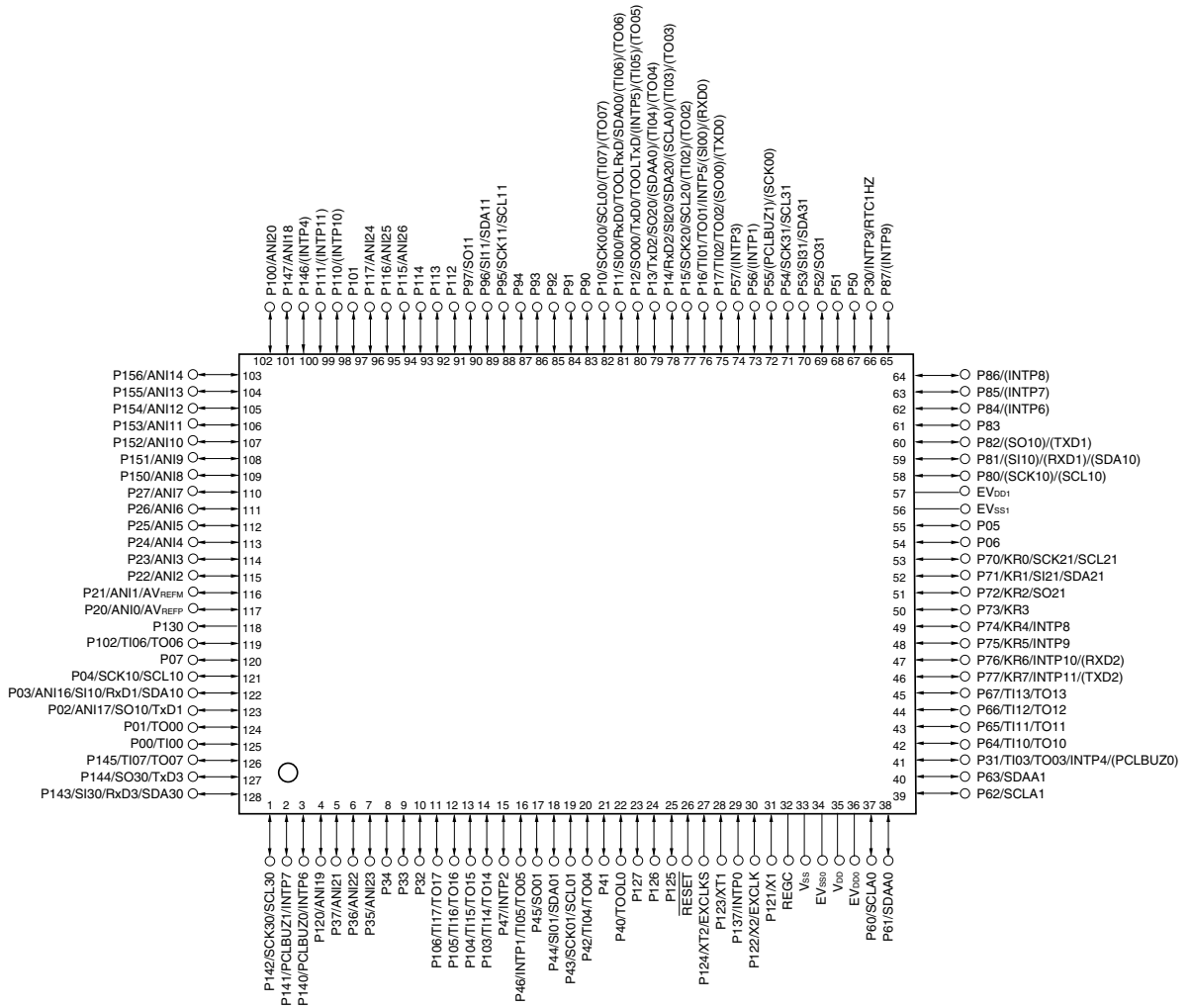


- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.14 128-pin products

- 128-pin plastic LQFP (fine pitch) (14 × 20)



- Cautions**
1. Make EV_{SS0}, EV_{SS1} pins the same potential as V_{SS} pin.
 2. Make V_{DD} pin the potential that is higher than EV_{DD0}, EV_{DD1} pins (EV_{DD0} = EV_{DD1}).
 3. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

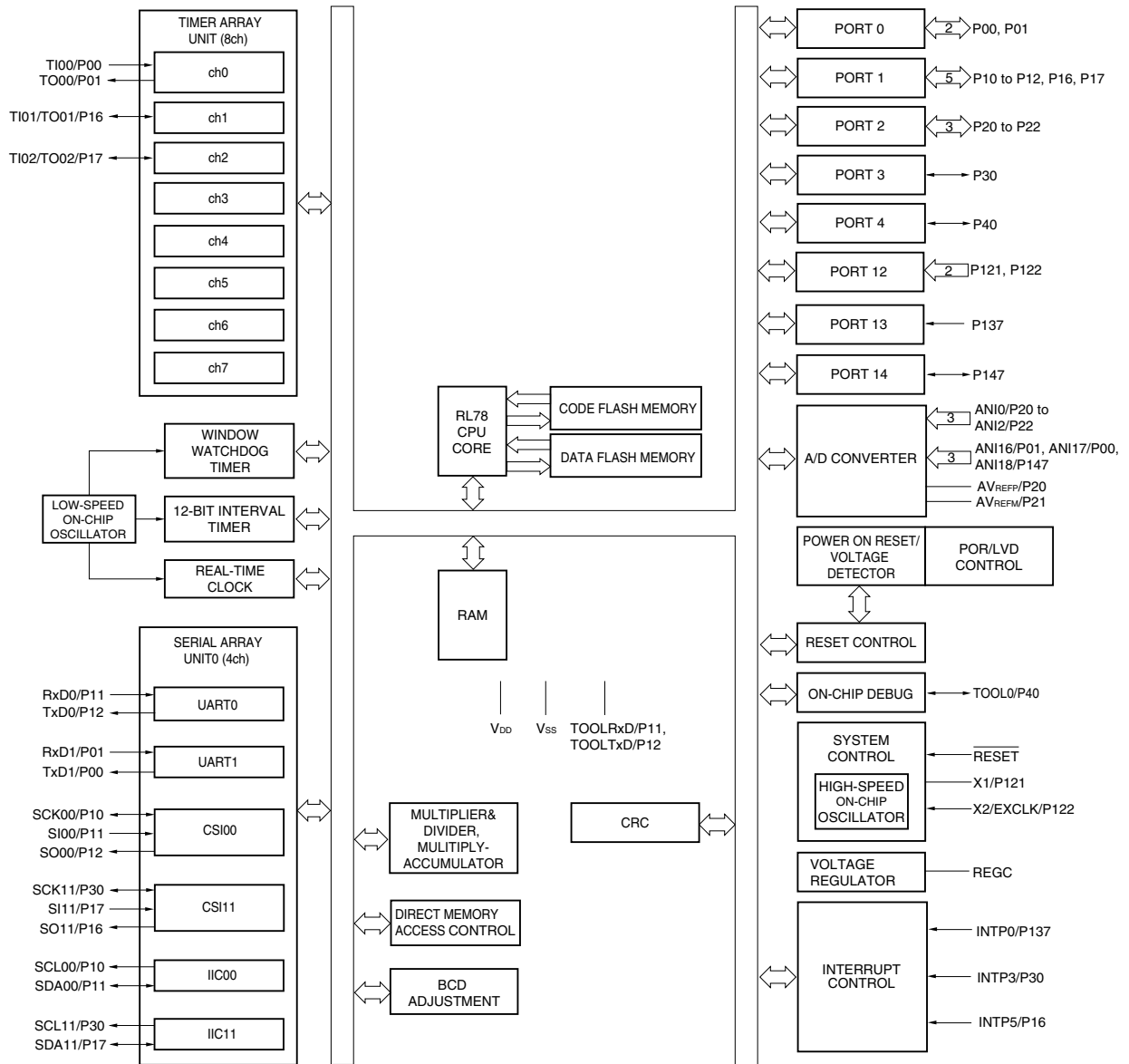
- Remarks**
1. For pin identification, see 1.4 Pin Identification.
 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0} and EV_{DD1} pins and connect the V_{SS}, EV_{SS0} and EV_{SS1} pins to separate ground lines.
 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

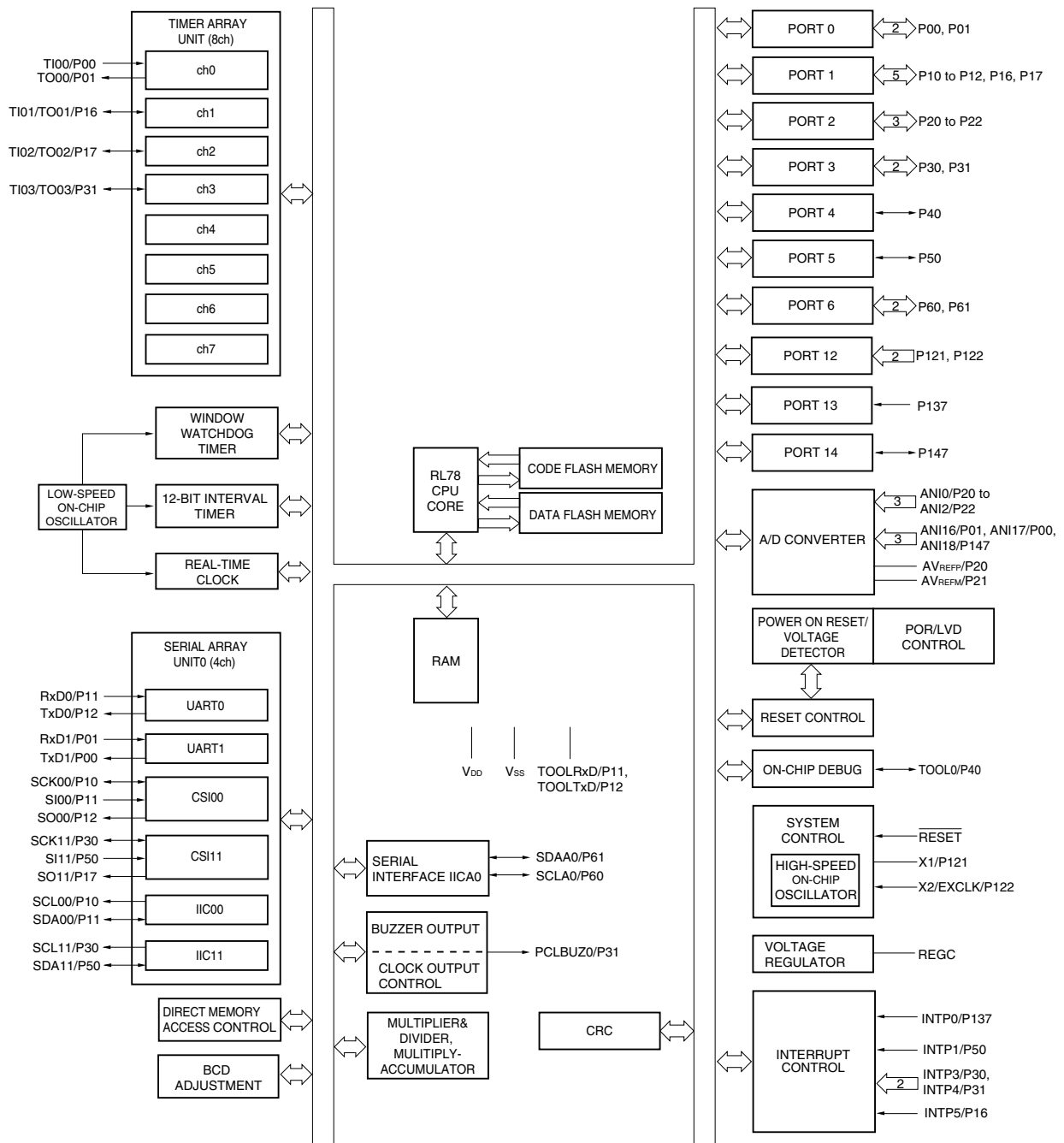
ANI0 to ANI14,		REGC:	Regulator capacitance
ANI16 to ANI26:	Analog input	RESET:	Reset
AVREFM:	A/D converter reference potential (– side) input	RTC1HZ:	Real-time clock correction clock (1 Hz) output
AVREFP:	A/D converter reference potential (+ side) input	RxD0 to RxD3:	Receive data
EVDD0, EVDD1:	Power supply for port	SCK00, SCK01, SCK10, SCK11, SCK20, SCK21,	
EVSS0, EVSS1:	Ground for port	SCK30, SCK31:	Serial clock input/output
EXCLK:	External clock input (Main system clock)	SCLA0, SCLA1, SCL00, SCL01, SCL10, SCL11,	
EXCLKS:	External clock input (Subsystem clock)	SCL20, SCL21, SCL30, SCL31:	Serial clock output
<R> INTP0 to INTP11:	Interrupt request from peripheral	SDAA0, SDAA1, SDA00, SDA01, SDA10, SDA11, SDA20, SDA21, SDA30, SDA31:	Serial data input/output
KR0 to KR7:	Key return	SI00, SI01, SI10, SI11, SI20, SI21, SI30, SI31:	Serial data input
P00 to P07:	Port 0	SO00, SO01, SO10, SO11, SO20, SO21, SO30, SO31:	Serial data output
P10 to P17:	Port 1	TI00 to TI07, TI10 to TI17:	Timer input
P20 to P27:	Port 2	TO00 to TO07, TO10 to TO17:	Timer output
P30 to P37:	Port 3	TOOL0:	Data input/output for tool
P40 to P47:	Port 4	TOOLRxD, TOOLTxD:	Data input/output for external device
P50 to P57:	Port 5	TxD0 to TxD3:	Transmit data
P60 to P67:	Port 6	V _{DD} :	Power supply
P70 to P77:	Port 7	V _{SS} :	Ground
P80 to P87:	Port 8	X1, X2:	Crystal oscillator (main system clock)
P90 to P97:	Port 9	XT1, XT2:	Crystal oscillator (subsystem clock)
P100 to P106:	Port 10		
P110 to P117:	Port 11		
P120 to P127:	Port 12		
P130, P137:	Port 13		
P140 to P147:	Port 14		
P150 to P156:	Port 15		
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output		

1.5 Block Diagram

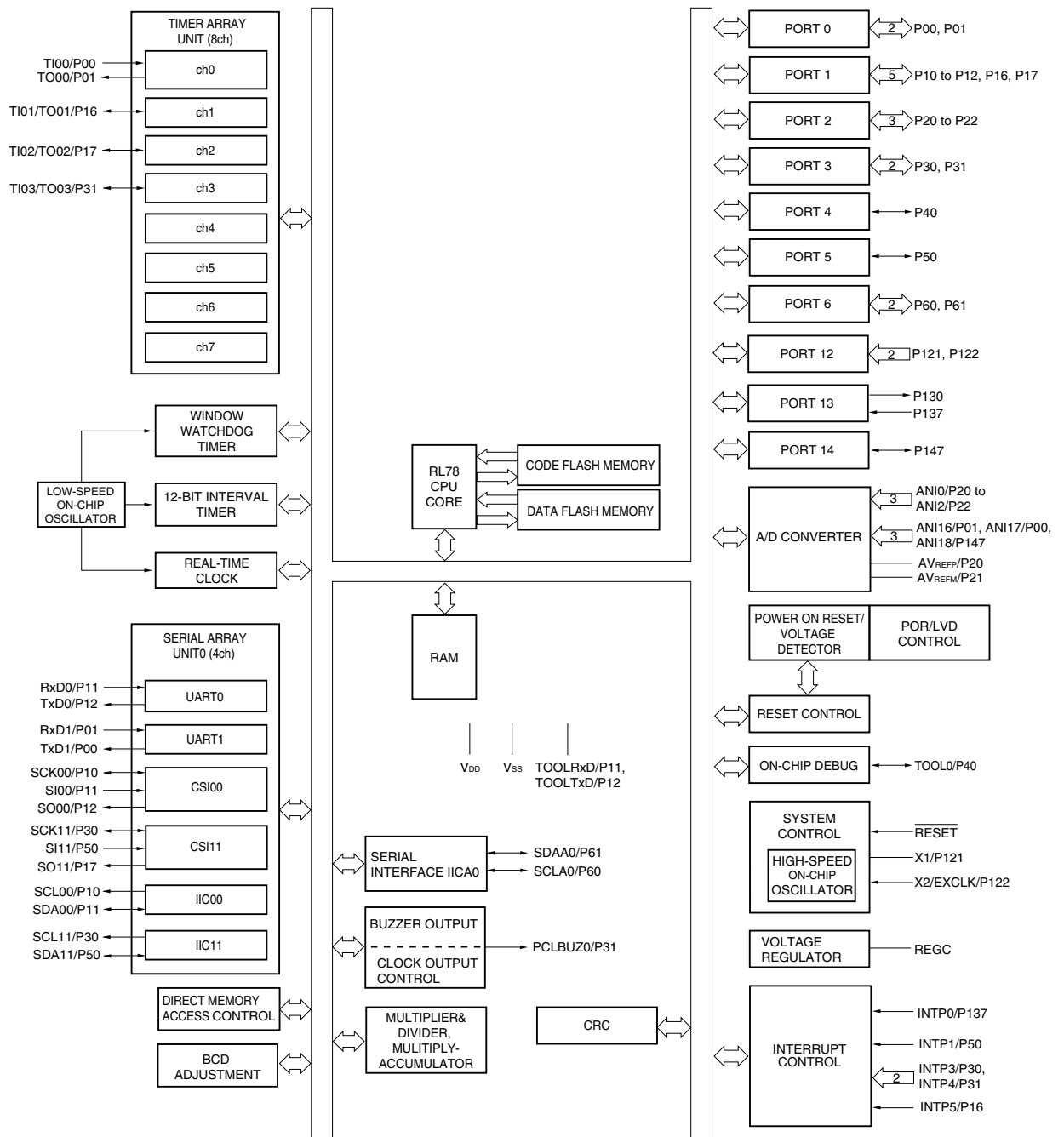
1.5.1 20-pin products



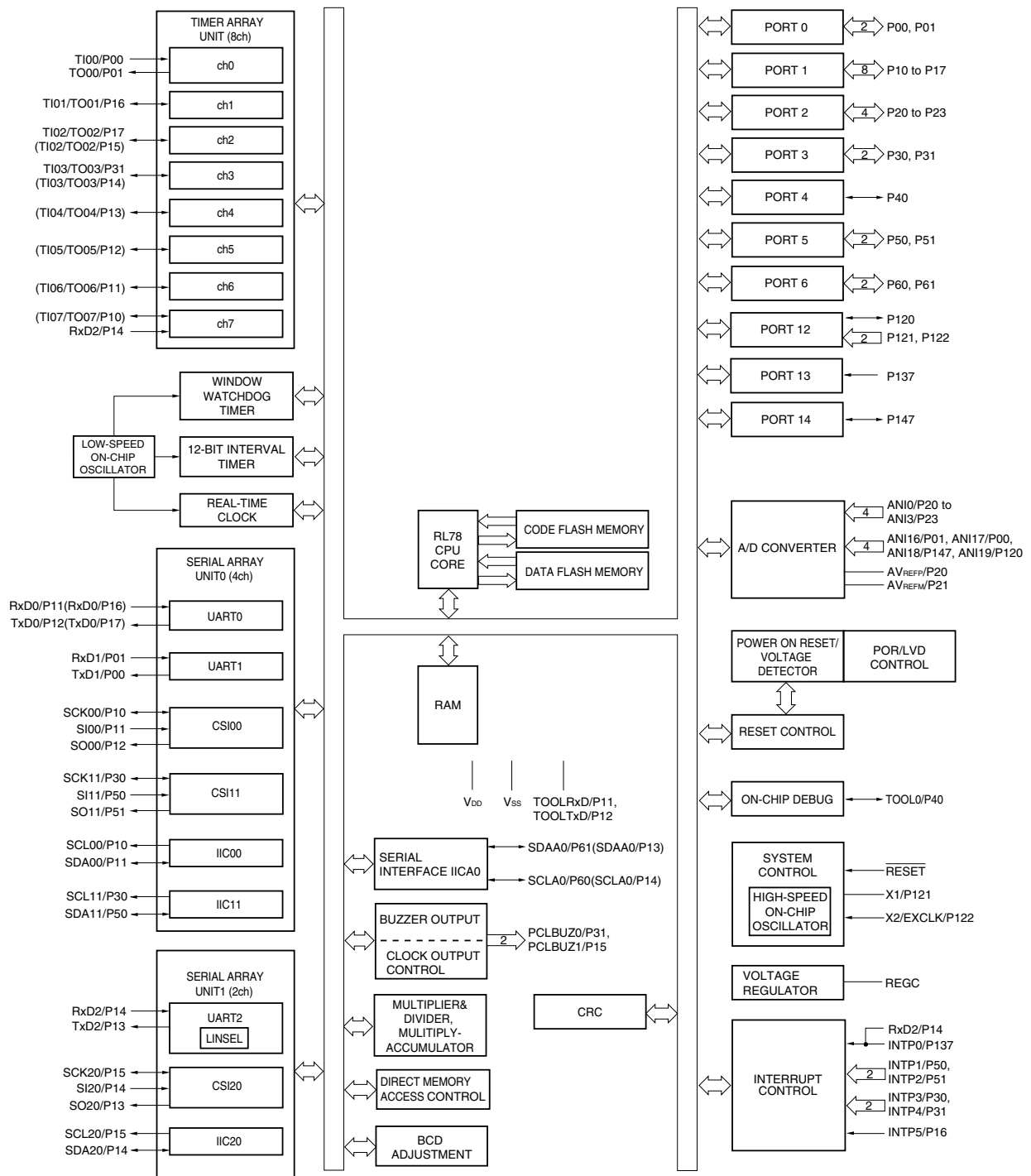
1.5.2 24-pin products



1.5.3 25-pin products

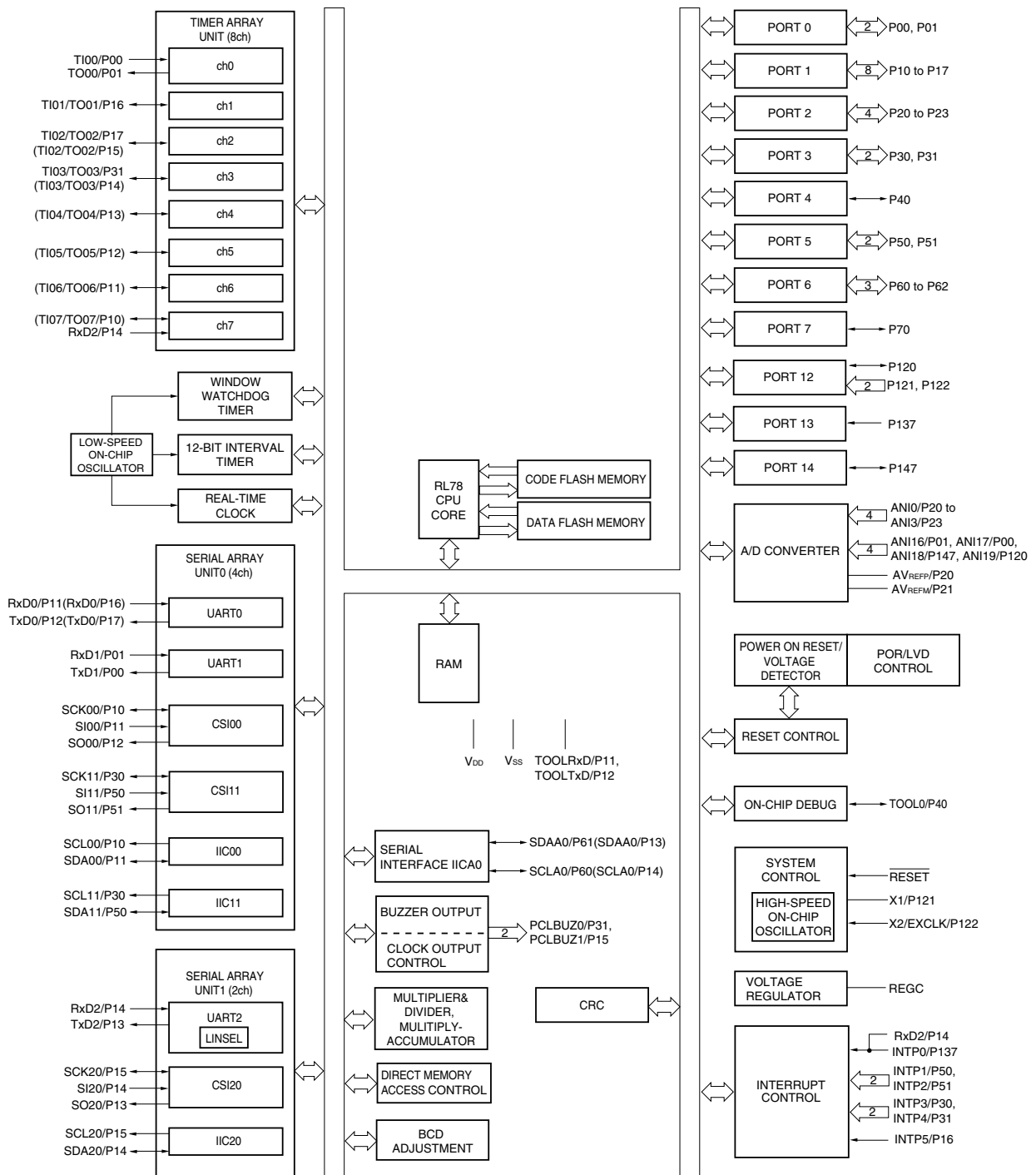


1.5.4 30-pin products



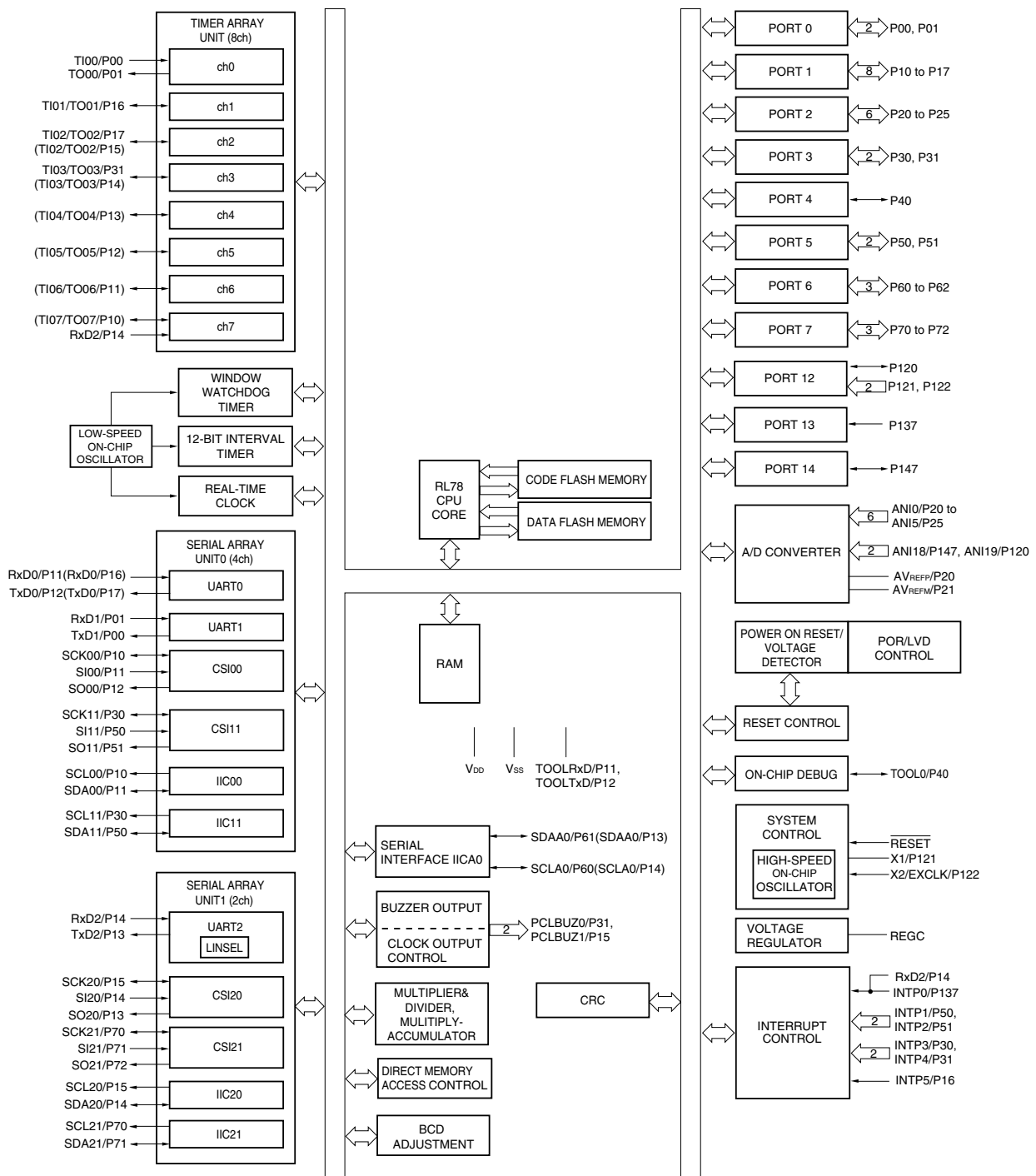
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.5 32-pin products



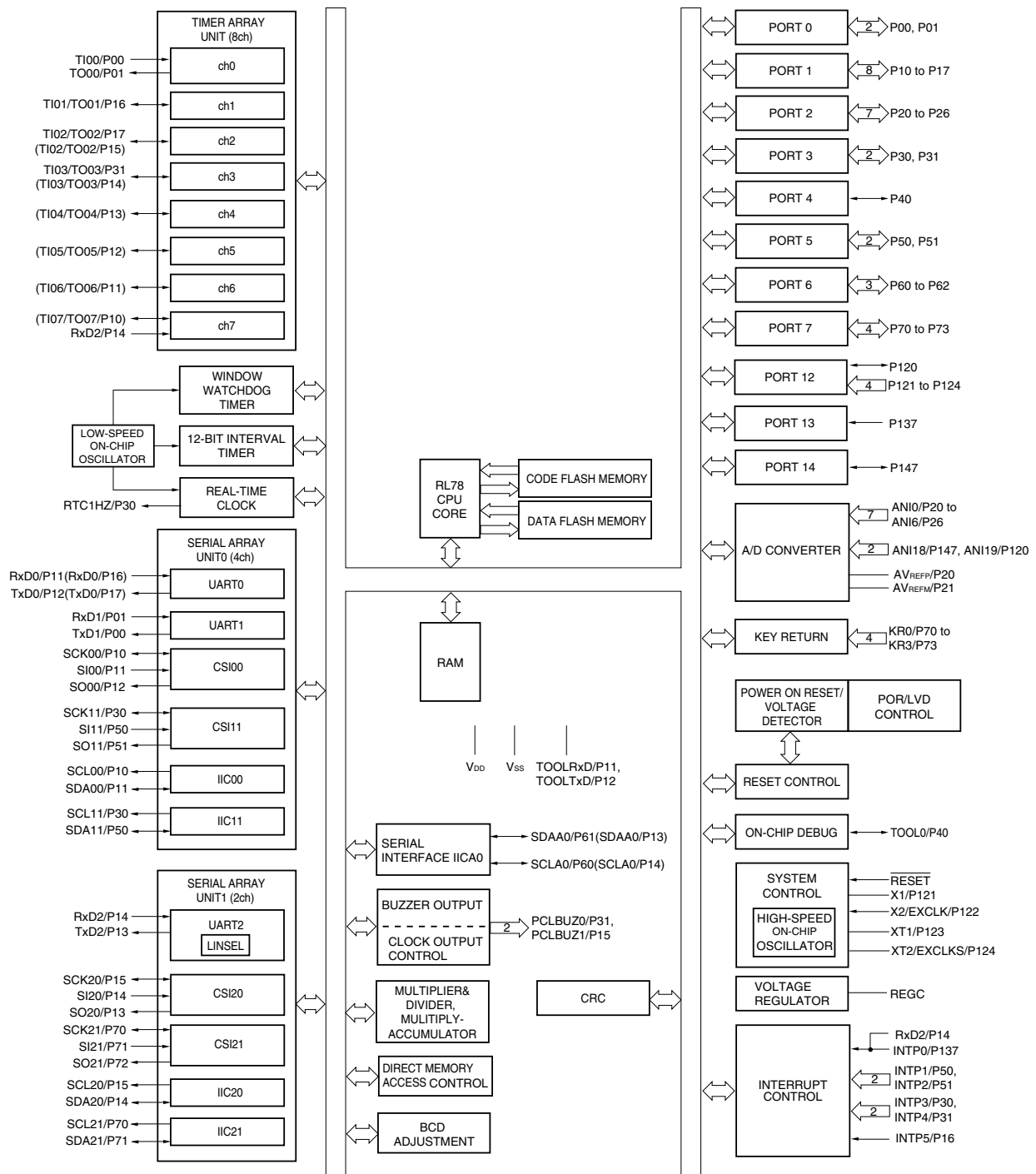
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.6 36-pin products



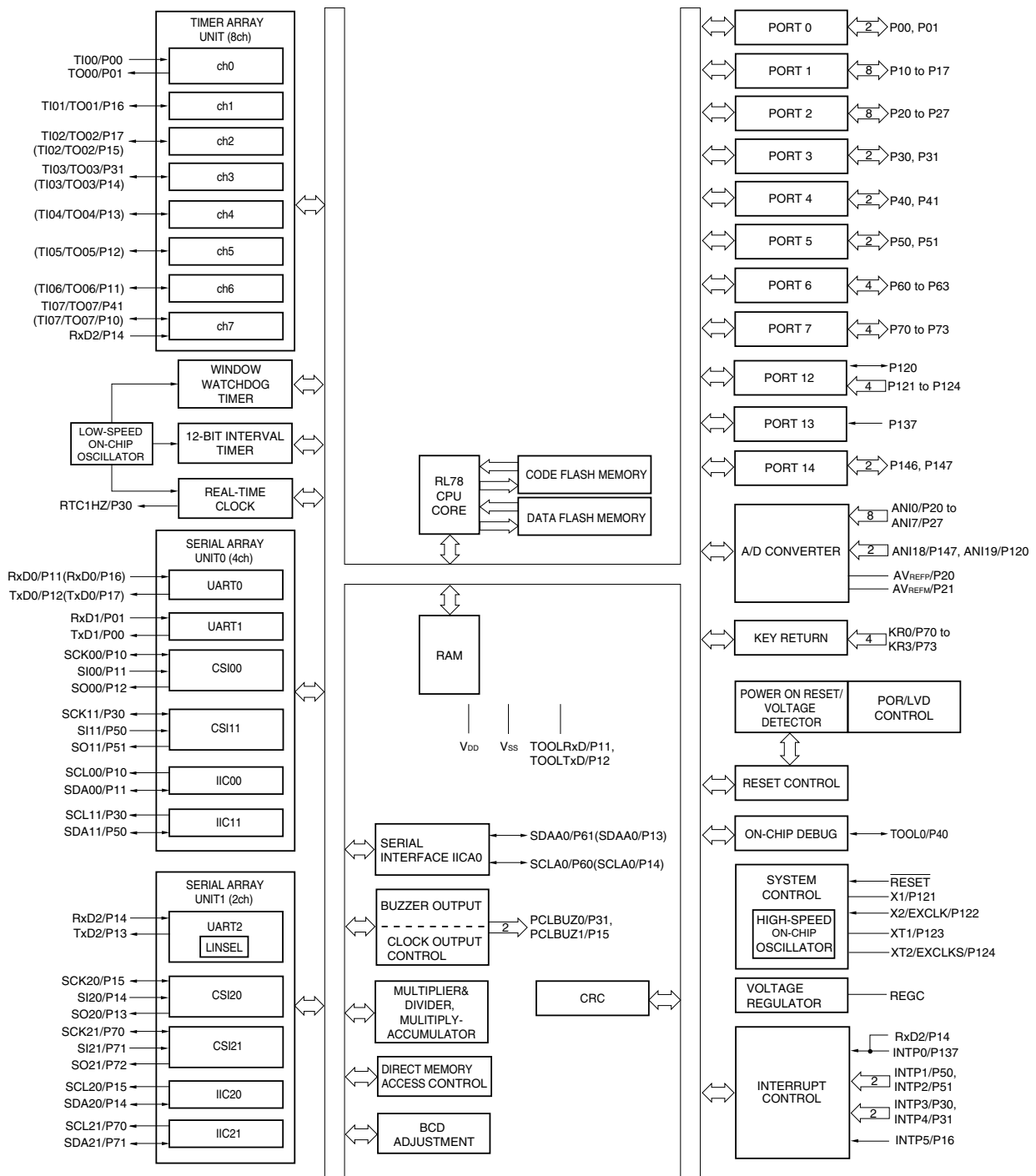
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.7 40-pin products



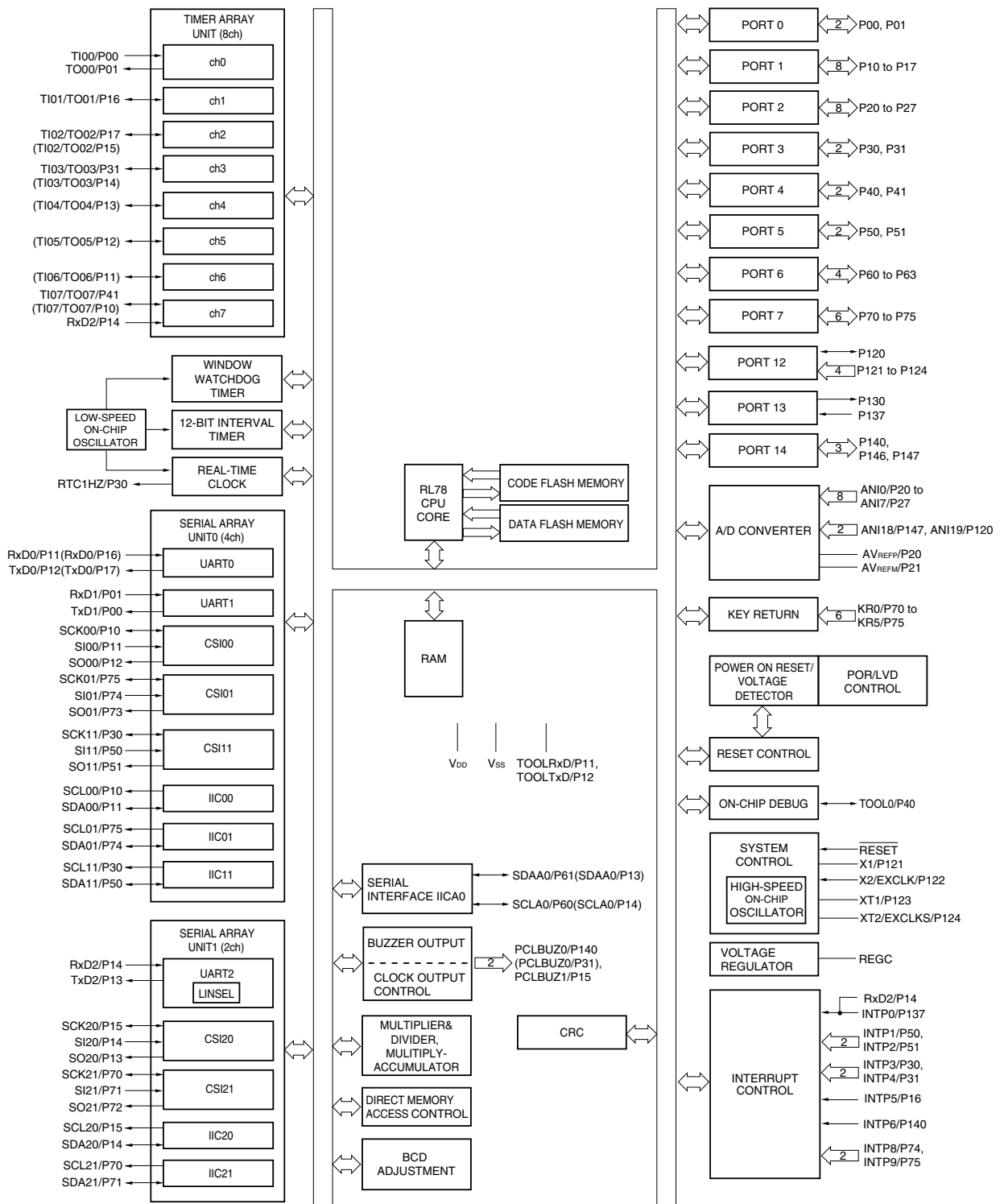
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.8 44-pin products



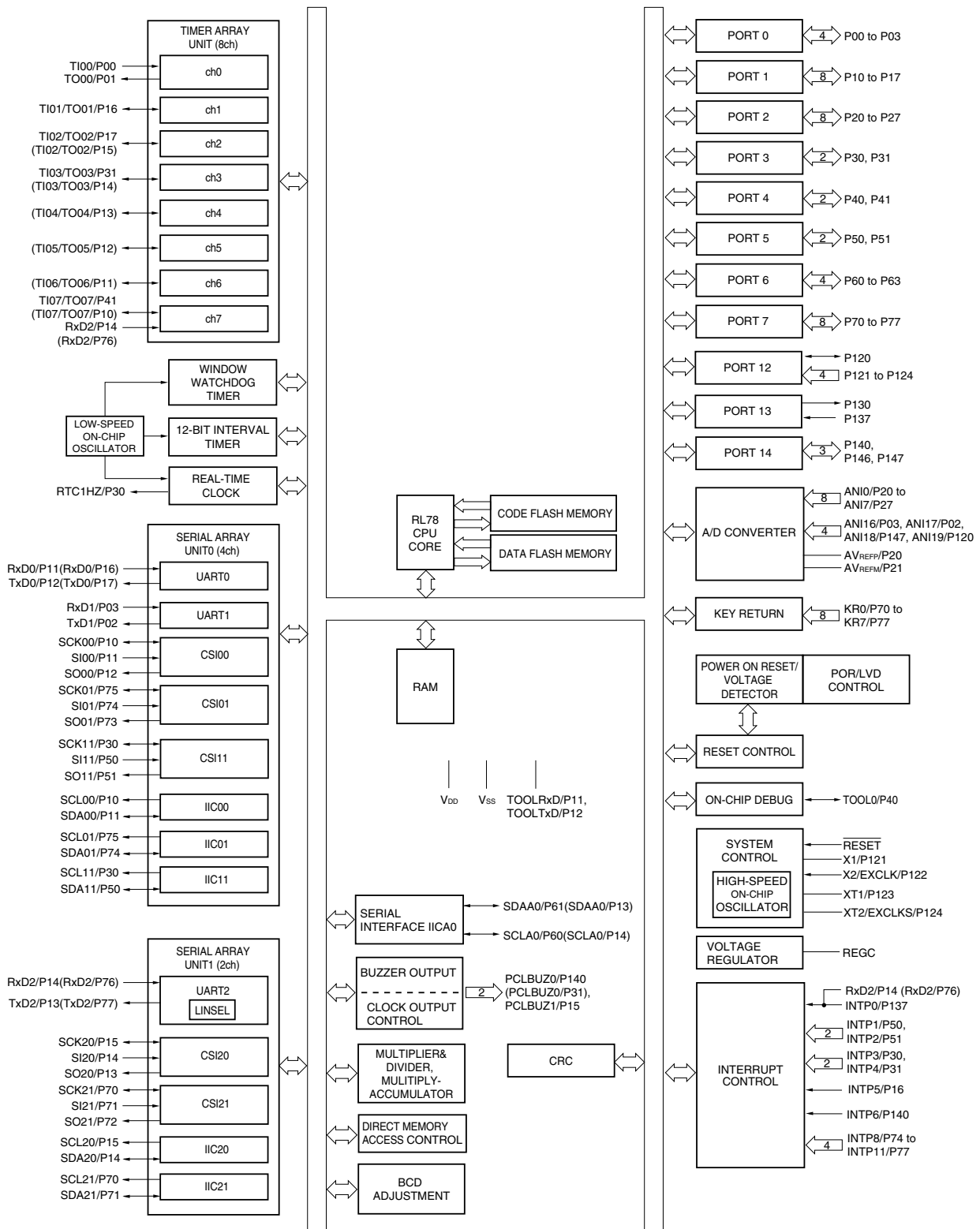
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.9 48-pin products



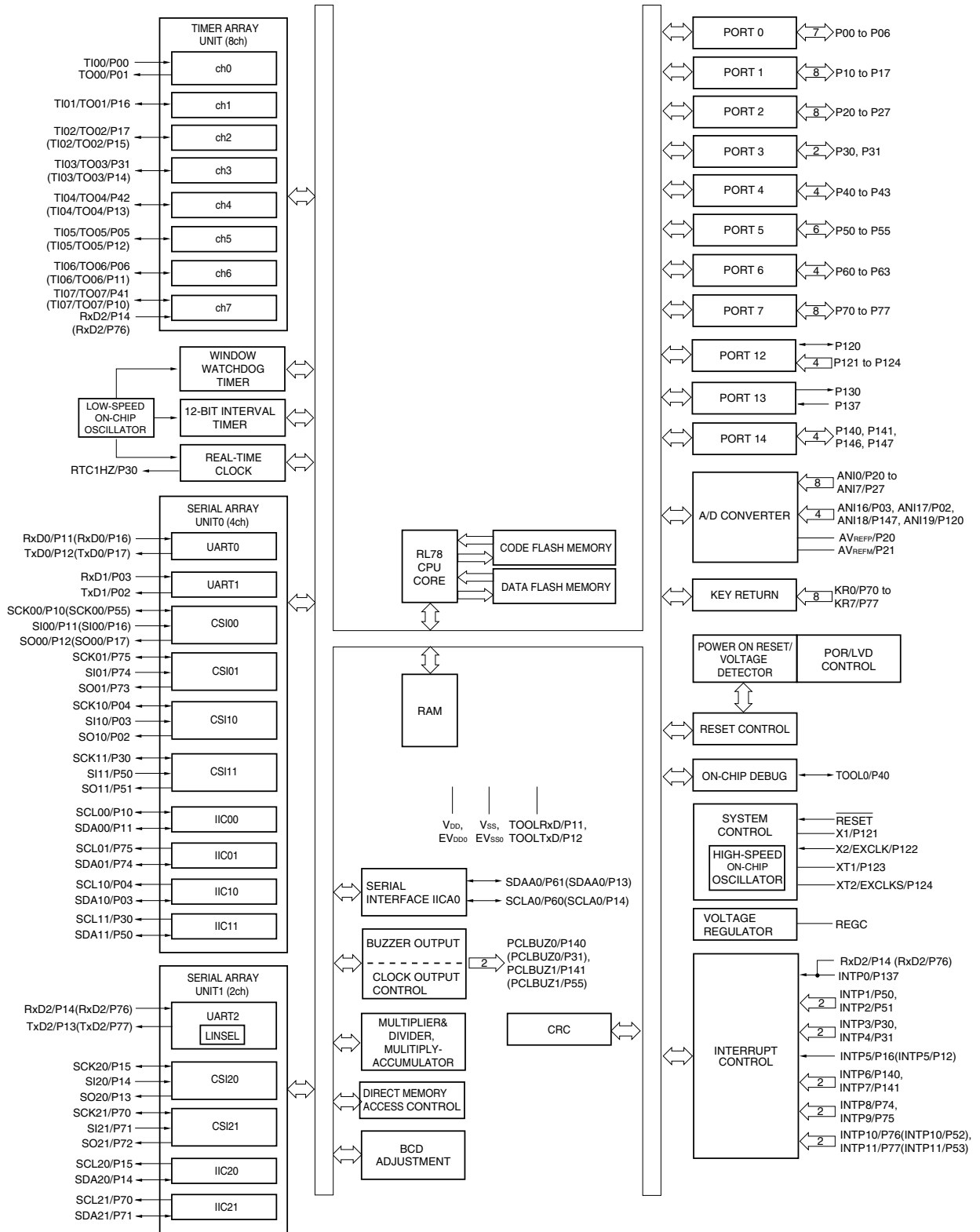
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.10 52-pin products



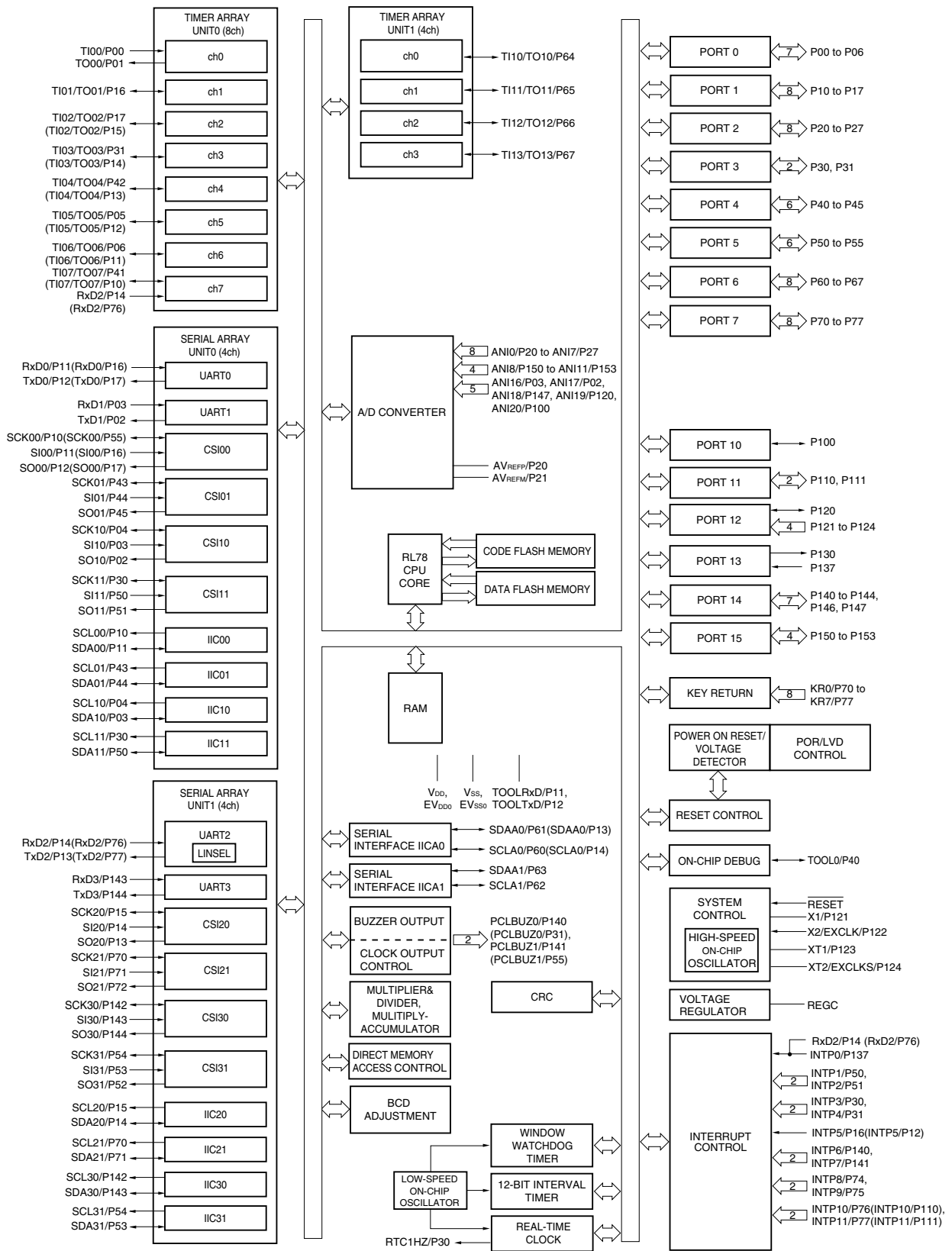
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.11 64-pin products



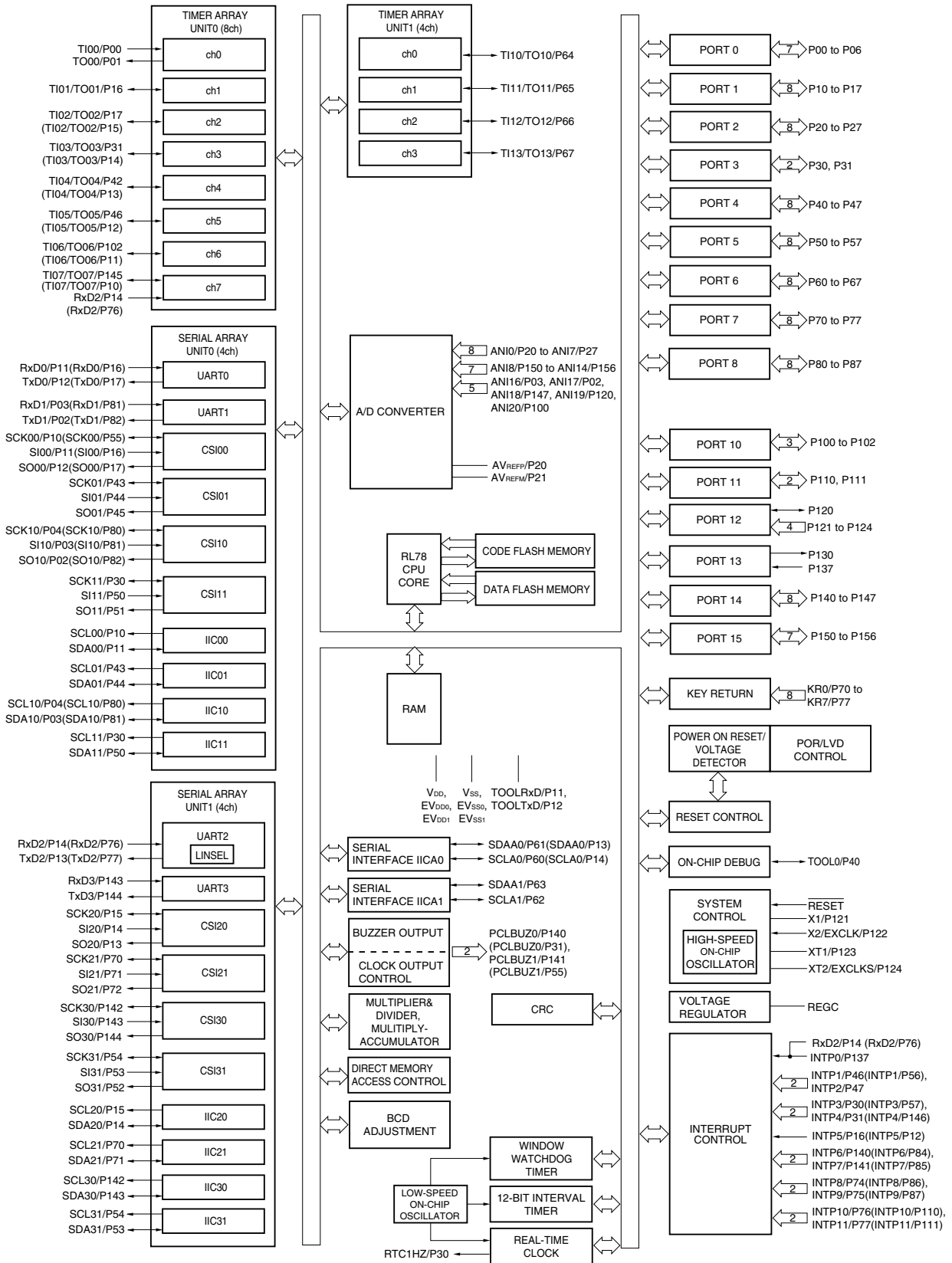
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.12 80-pin products



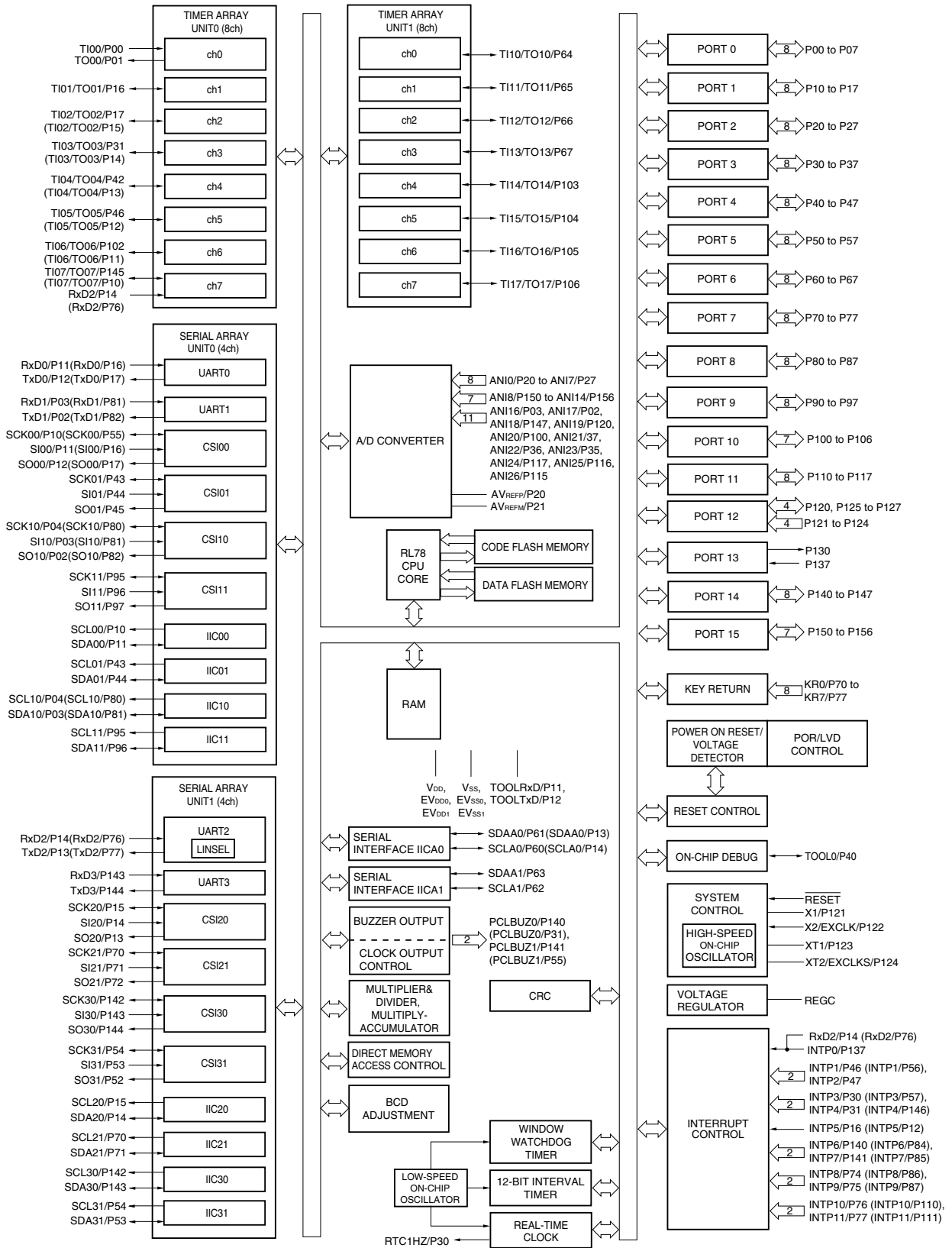
Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.13 100-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.5.14 128-pin products



Remark Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.6 Outline of Functions

[20-pin, 24-pin, 25-pin, 30-pin, 32-pin, 36-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H other than timer output.

(1/2)

Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin	
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx
Code flash memory (KB)	16 to 64		16 to 64		16 to 64		16 to 128		16 to 128		16 to 128	
Data flash memory (KB)	4	–	4	–	4	–	4 to 8	–	4 to 8	–	4 to 8	–
RAM (KB)	2 to 4 ^{Note1}		2 to 4 ^{Note1}		2 to 4 ^{Note1}		2 to 12 ^{Note1}		2 to 12 ^{Note1}		2 to 12 ^{Note1}	
Memory space	1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V										
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)										
Subsystem clock	–											
Low-speed on-chip oscillator	15 kHz (TYP.)											
General-purpose register	(8-bit register × 8) × 4 banks											
Minimum instruction execution time	0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation)											
	0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)											
Instruction set	<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 											
I/O port	Total	16	20	21	26	28	32					
	CMOS I/O	13	15	15	21	22	26					
	CMOS input	3	3	3	3	3	3					
	CMOS output	–	–	1	–	–	–					
	N-ch O.D I/O (6 V tolerance)	–	2	2	2	3	3					
Timer	16-bit timer	8 channels										
	Watchdog timer	1 channel										
	Real-time clock (RTC)	1 channel										
	12-bit interval timer (IT)	1 channel										
	Timer output	3 channels (PWM outputs: 2 ^{Note2})	4 channels (PWM outputs: 3 ^{Note2})				4 channels (PWM outputs: 3 ^{Note2}), 8 channels ^{Note3} (PWM outputs: 7 ^{Note2})					
	RTC output	–										

- Notes**
1. In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used.
 2. The number of outputs varies, depending on the setting of channels in use and the number of the master.
 3. When setting to PIOR = 1

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(2/2)

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Item	20-pin		24-pin		25-pin		30-pin		32-pin		36-pin		
	R5F1006x	R5F1016x	R5F1007x	R5F1017x	R5F1008x	R5F1018x	R5F100Ax	R5F101Ax	R5F100Bx	R5F101Bx	R5F100Cx	R5F101Cx	
Clock output/buzzer output	-		1		1		2		2		2		
	<ul style="list-style-type: none"> 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)												
8/10-bit resolution A/D converter	6 channels		6 channels		6 channels		8 channels		8 channels		8 channels		
Serial interface	[20-pin, 24-pin, 25-pin products] <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel [30-pin, 32-pin products] <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-pin products] <ul style="list-style-type: none"> CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel CSI: 2 channel/simplified I²C: 2 channel/UART (UART supporting LIN-bus): 1 channel 												
	I ² C bus	-		1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	<ul style="list-style-type: none"> 16 bits × 16 bits = 32 bits (Unsigned or signed) 32 bits ÷ 32 bits = 32 bits (Unsigned) 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) 												
DMA controller	2 channels												
Vectored interrupt sources	Internal	23		24		24		27		27		27	
	External	3		5		5		6		6		6	
Key interrupt	-												
Reset	<ul style="list-style-type: none"> Reset by RESET pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access 												
Power-on-reset circuit	<ul style="list-style-type: none"> Power-on-reset: 1.51 ±0.03 V Power-down-reset: 1.50 ±0.03 V 												
Voltage detector	<ul style="list-style-type: none"> Rising edge : 1.67 V to 4.06 V (14 stages) Falling edge : 1.63 V to 3.98 V (14 stages) 												
On-chip debug function	Provided												
Power supply voltage	V _{DD} = 1.6 to 5.5 V												
Operating ambient temperature	T _A = -40 to +85 °C												

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[40-pin, 44-pin, 48-pin, 52-pin, 64-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H other than timer output.

(1/2)

Item		40-pin		44-pin		48-pin		52-pin		64-pin			
		R5F100EX	R5F101EX	R5F100FX	R5F101FX	R5F100GX	R5F101GX	R5F100JX	R5F101JX	R5F100LX	R5F101LX		
Code flash memory (KB)		16 to 192		16 to 512		16 to 512		32 to 512		32 to 512			
Data flash memory (KB)		4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–	4 to 8	–		
RAM (KB)		2 to 16 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}		2 to 32 ^{Note1}			
Memory space		1 MB											
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V											
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)											
<R>	Subsystem clock	XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz											
<R>	Low-speed on-chip oscillator	15 kHz (TYP.)											
<R>	General-purpose register	(8-bit register × 8) × 4 banks											
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f _{IH} = 32 MHz operation)											
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)											
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)											
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 											
I/O port	Total	36	40	44	48	58							
	CMOS I/O	28	31	34	38	48							
	CMOS input	5	5	5	5	5							
	CMOS output	–	–	1	1	1							
	N-ch O.D I/O (6 V tolerance)	3	4	4	4	4							
Timer	16-bit timer	8 channels											
	Watchdog timer	1 channel											
	Real-time clock (RTC)	1 channel											
	12-bit interval timer (IT)	1 channel											
	Timer output	4 channels (PWM outputs: 3 ^{Note2}), 8 channels ^{Note3} (PWM outputs: 7 ^{Note2})	5 channels (PWM outputs: 4 ^{Note2}), 8 channels ^{Note3} (PWM outputs: 7 ^{Note2})							8 channels (PWM outputs: 7 ^{Note2})			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)											

- Notes**
- In the case of the 4 KB, this is about 3 KB when the self-programming function and data flash function are used.
In the case of the 20 KB, this is about 19 KB when the self-programming function and data flash function are used.
In the case of the 32 KB, this is about 31 KB when the self-programming function and data flash function are used.
 - The number of outputs varies, depending on the setting of channels in use and the number of the master.
 - When setting to PIOR = 1

(2/2)

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Item	40-pin		44-pin		48-pin		52-pin		64-pin		
	R5F100EX	R5F101EX	R5F100FX	R5F101FX	R5F100GX	R5F101GX	R5F100JX	R5F101JX	R5F100LX	R5F101LX	
Clock output/buzzer output	2		2		2		2		2		
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) 										
8/10-bit resolution A/D converter	9 channels		10 channels		10 channels		12 channels		12 channels		
Serial interface	[40-pin, 44-pin products] <ul style="list-style-type: none"> • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin, 52-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 1 channel/simplified I²C: 1 channel/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel 										
	I ² C bus	1 channel		1 channel		1 channel		1 channel		1 channel	
Multiplier and divider/multiply-accumulator	<ul style="list-style-type: none"> • 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) 										
DMA controller	2 channels										
Vectored interrupt sources	Internal	27		27		27		27		27	
	External	7		7		10		12		13	
Key interrupt	4		4		6		8		8		
Reset	<ul style="list-style-type: none"> • Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 										
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 										
Voltage detector	<ul style="list-style-type: none"> • Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages) 										
On-chip debug function	Provided										
Power supply voltage	V _{DD} = 1.6 to 5.5 V										
Operating ambient temperature	T _A = -40 to +85 °C										

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin, 128-pin products]

Caution This outline describes the functions at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

(1/2)

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Item		80-pin		100-pin		128-pin	
		R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Code flash memory (KB)		96 to 512		96 to 512		192 to 512	
Data flash memory (KB)		8	–	8	–	8	–
RAM (KB)		8 to 32 ^{Note 1}		8 to 32 ^{Note 1}		16 to 32 ^{Note 1}	
Memory space		1 MB					
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V _{DD} = 2.7 to 5.5 V, 1 to 8 MHz: V _{DD} = 1.8 to 2.7 V, 1 to 4 MHz: V _{DD} = 1.6 to 1.8 V					
	High-speed on-chip oscillator	HS (High-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (High-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (Low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (Low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)					
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz					
Low-speed on-chip oscillator		15 kHz (TYP.)					
General-purpose register		(8-bit register × 8) × 4 banks					
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator: f _H = 32 MHz operation)					
		0.05 μs (High-speed system clock: f _M = 20 MHz operation)					
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)					
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 					
I/O port	Total	74		92		120	
	CMOS I/O	64		82		110	
	CMOS input	5		5		5	
	CMOS output	1		1		1	
	N-ch O.D I/O (6 V tolerance)	4		4		4	
Timer	16-bit timer	12 channels		12 channels		16 channels	
	Watchdog timer	1 channel		1 channel		1 channel	
	Real-time clock (RTC)	1 channel		1 channel		1 channel	
	12-bit interval timer (IT)	1 channel		1 channel		1 channel	
	Timer output	12 channels (PWM outputs: 10 ^{Note 2})		12 channels (PWM outputs: 10 ^{Note 2})		16 channels (PWM outputs: 14 ^{Note 2})	
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)					

- Notes**
- In the case of the 20 KB, this is about 19 KB when the self-programming function and data flash function are used.
In the case of the 32 KB, this is about 31 KB when the self-programming function and data flash function are used.
 - The number of outputs varies, depending on the setting of channels in use and the number of the master

(2/2)

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Item	80-pin		100-pin		128-pin	
	R5F100Mx	R5F101Mx	R5F100Px	R5F101Px	R5F100Sx	R5F101Sx
Clock output/buzzer output	2		2		2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) 					
8/10-bit resolution A/D converter	17 channels		20 channels		26 channels	
Serial interface	[80-pin, 100-pin, 128-pin products]					
	<ul style="list-style-type: none"> • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • CSI: 2 channels/simplified I²C: 2 channels/UART: 1 channel 					
I ² C bus	2 channel		2 channel		2 channel	
Multiplier and divider/multiply-accumulator	<ul style="list-style-type: none"> • 16 bits × 16 bits = 32 bits (Unsigned or signed) • 32 bits ÷ 32 bits = 32 bits (Unsigned) • 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed) 					
DMA controller	4 channels					
Vectored interrupt sources	Internal	37		37		41
	External	13		13		13
Key interrupt	8		8		8	
Reset	<ul style="list-style-type: none"> • Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 					
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 					
Voltage detector	<ul style="list-style-type: none"> • Rising edge : 1.67 V to 4.06 V (14 stages) • Falling edge : 1.63 V to 3.98 V (14 stages) 					
On-chip debug function	Provided					
Power supply voltage	$V_{DD} = 1.6$ to 5.5 V					
Operating ambient temperature	$T_A = -40$ to +85 °C					

Note The illegal instruction is generated when instruction code FFH is executed.

Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

- Cautions**
1. The RL78/G13 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.
 2. With products not provided with an EV_{DD0} , EV_{DD1} , EV_{SS0} , or EV_{SS1} pin, replace EV_{DD0} and EV_{DD1} with V_{DD} , or replace EV_{SS0} and EV_{SS1} with V_{SS} .
 3. The pins mounted depend on the product. Refer to 1.3.1 20-pin products to 1.3.14 128-pin products.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	V _{SS}		-0.5 to +0.3	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 ^{Note 1}	V
Input voltage	V _{I1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 ^{Note 2}	V
Output voltage	V _{O1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 ^{Note 2}	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3 ^{Note 2}	V
Analog input voltage	V _{AI1}	ANI16 to ANI26	-0.3 to EV _{DD0} +0.3 and -0.3 to AV _{REF(+)} +0.3 ^{Notes 2, 3}	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF(+)} +0.3 ^{Notes 2, 3}	V

Notes 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

2. Must be 6.5 V or lower.

3. Do not exceed AV_{REF(+)} + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. AV_{REF(+)} : + side reference voltage of the A/D converter.

Absolute Maximum Ratings (TA = 25°C) (2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

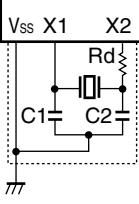
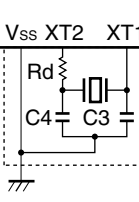
Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 oscillator characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq E_{V_{DD0}} = E_{V_{DD1}} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = E_{V_{SS0}} = E_{V_{SS1}} = 0\text{ V}$)

Parameter	Resonator	Recommended Circuit	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (f_x) ^{Note}	Ceramic resonator/ crystal resonator		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1.0		20.0	MHz
			$1.8\text{ V} \leq V_{DD} < 2.7\text{ V}$	1.0		8.0	MHz
			$1.6\text{ V} \leq V_{DD} < 1.8\text{ V}$	1.0		4.0	MHz
XT1 clock oscillation frequency (f_x) ^{Note}	Crystal resonator			32	32.768	35	kHz

Note Indicates only oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Cautions 1. When using the X1 oscillator, XT1 oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- Keep the wiring length as short as possible.
 - Do not cross the wiring with the other signal lines.
 - Do not route the wiring near a signal line through which a high fluctuating current flows.
 - Always make the ground point of the oscillator capacitor the same potential as V_{SS} .
 - Do not ground the capacitor to a ground pattern through which a high current flows.
 - Do not fetch signals from the oscillator.
2. Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.
 3. The XT1 oscillator is designed as a low-amplitude circuit for reducing power consumption, and is more prone to malfunction due to noise than the X1 oscillator. Particular care is therefore required with the wiring method when the XT1 clock is used.

2.2.2 On-chip oscillator characteristics

(T_A = -40 to +85°C, 1.6 V ≤ E_{VDD0} = E_{VDD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = E_{VSS0} = E_{VSS1} = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Note 1}	f _H			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy ^{Note 2}		-20 to +85 °C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1		+1	%
			1.6 V ≤ V _{DD} < 1.8 V	-5		+5	%
		-40 to -20 °C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5		+1.5	%
			1.6 V ≤ V _{DD} < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _L				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 3 of option byte (000C2H/010C2H) and bits 0 to 2 of HOCODIV register.

2. This indicates the oscillator characteristics only. Refer to AC Characteristics for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EVDD0 ≤ 5.5 V			-10.0 ^{Note 2}	mA	
			Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty = 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-55.0	mA
				2.7 V ≤ EVDD0 < 4.0 V			-10.0	mA
				1.8 V ≤ EVDD0 < 2.7 V			-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty = 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-80.0	mA	
			2.7 V ≤ EVDD0 < 4.0 V			-19.0	mA	
			1.8 V ≤ EVDD0 < 2.7 V			-10.0	mA	
			1.6 V ≤ EVDD0 < 1.8 V			-5.0	mA	
		Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ EVDD0 ≤ 5.5 V			-135.0 ^{Note 4}	mA	
		IOH2	Per pin for P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V			-0.1 ^{Note 2}	mA
				Total of all pins (When duty = 70% ^{Note 3})	1.6 V ≤ VDD ≤ 5.5 V			-1.5

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
 - Total output current of pins = $(I_{OH} \times 0.7) / (n \times 0.01)$
 <Example> Where n = 50% and IOH = -10.0 mA
 Total output current of pins = $(-10.0 \times 0.7) / (50 \times 0.01) = -14.0$ mA
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.
 - The applied current for the products for industrial application (R5F100xxDxx, R5F101xxDxx) is -100 mA.

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**(2/5)**

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, I_{OL} ^{Note 1}	I _{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			20.0 ^{Note 2}	mA	
		Per pin for P60 to P63			15.0 ^{Note 2}	mA	
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			70.0	mA
			$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$			15.0	mA
			$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$			9.0	mA
			$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (When duty = 70% ^{Note 3})	$4.0\text{ V} \leq \text{EV}_{\text{DD}0} \leq 5.5\text{ V}$			80.0	mA
	$2.7\text{ V} \leq \text{EV}_{\text{DD}0} < 4.0\text{ V}$				35.0	mA	
	$1.8\text{ V} \leq \text{EV}_{\text{DD}0} < 2.7\text{ V}$				20.0	mA	
	$1.6\text{ V} \leq \text{EV}_{\text{DD}0} < 1.8\text{ V}$				10.0	mA	
Total of all pins (When duty = 70% ^{Note 3})				150.0	mA		
I _{OL2}	Per pin for P20 to P27, P150 to P156				0.4 ^{Note 2}	mA	
	Total of all pins (When duty = 70% ^{Note 3})	$1.6\text{ V} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$			5.0	mA	

- Notes**
- Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EV_{SS0}, EV_{SS1} and V_{SS} pin.
 - However, do not exceed the total current value.
 - Specification under conditions where the duty factor is 70%.
The output current value that has changed the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).
 - Total output current of pins = $(\text{I}_{\text{OL}} \times 0.7) / (n \times 0.01)$
<Example> Where n = 50% and I_{OL} = 10.0 mA
Total output current of pins = $(10.0 \times 0.7) / (50 \times 0.01) = 14.0\text{ mA}$
 However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8EV _{DD0}		EV _{DD0}	V
	V _{IH2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	2.2		EV _{DD0}	V
			TTL input buffer 3.3 V ≤ EV _{DD0} < 4.0 V	2.0		EV _{DD0}	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	1.5		EV _{DD0}	V
	V _{IH3}	P20 to P27, P150 to P156		0.7V _{DD}		V _{DD}	V
	V _{IH4}	P60 to P63		0.7EV _{DD0}		6.0	V
	V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8V _{DD}		V _{DD}	V
Input voltage, low	V _{IL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2EV _{DD0}	V
	V _{IL2}	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EV _{DD0} ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EV _{DD0} < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EV _{DD0} < 3.3 V	0		0.32	V
	V _{IL3}	P20 to P27, P150 to P156		0		0.3V _{DD}	V
	V _{IL4}	P60 to P63		0		0.3EV _{DD0}	V
	V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2V _{DD}	V

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 is EV_{DD0}, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	V _{OH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -10.0 mA	EV _{DD0} - 1.5		V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -3.0 mA	EV _{DD0} - 0.7		V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -2.0 mA	EV _{DD0} - 0.6		V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OH1} = -1.5 mA	EV _{DD0} - 0.5		V
			1.6 V ≤ EV _{DD0} < 1.8 V, I _{OH1} = -1.0 mA	EV _{DD0} - 0.5		V
	V _{OH2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OH2} = -100 μA	V _{DD} - 0.5		V
Output voltage, low	V _{OL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 20 mA		1.3	V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 8.5 mA		0.7	V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 3.0 mA		0.6	V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 1.5 mA		0.4	V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL1} = 0.6 mA		0.4	V
			1.6 V ≤ EV _{DD0} < 5.5 V, I _{OL1} = 0.3 mA		0.4	V
			V _{OL2}	P20 to P27, P150 to P156	1.6 V ≤ V _{DD} ≤ 5.5 V, I _{OL2} = 400 μA	
	V _{OL3}	P60 to P63	4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 15.0 mA		2.0	V
			4.0 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 5.0 mA		0.4	V
			2.7 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 3.0 mA		0.4	V
			1.8 V ≤ EV _{DD0} ≤ 5.5 V, I _{OL3} = 2.0 mA		0.4	V
			1.6 V ≤ EV _{DD0} < 5.5 V, I _{OL3} = 1.0 mA		0.4	V

Caution P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input leakage current, high	I _{LH1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{DD0}			1	μA
	I _{LH2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{DD}			1	μA
	I _{LH3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{DD}	In input port or external clock input			1
			In resonator connection			10	μA
Input leakage current, low	I _{LIL1}	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0}			-1	μA
	I _{LIL2}	P20 to P27, P137, P150 to P156, RESET	V _I = V _{SS}			-1	μA
	I _{LIL3}	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	V _I = V _{SS}	In input port or external clock input			-1
			In resonator connection			-10	μA
On-chip pull-up resistance	R _U	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	V _I = EV _{SS0} , In input port	10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current	IDD1 ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V	2.1		mA
						V _{DD} = 3.0 V	2.1		mA
					Normal operation	V _{DD} = 5.0 V	4.6	7.0	mA
				V _{DD} = 3.0 V		4.6	7.0	mA	
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V	3.7	5.5	mA
						V _{DD} = 3.0 V	3.7	5.5	mA
			Normal operation		V _{DD} = 5.0 V	2.7	4.0	mA	
				V _{DD} = 3.0 V	2.7	4.0	mA		
			LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V	1.2	1.8	mA
						V _{DD} = 2.0 V	1.2	1.8	mA
			LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V	1.2	1.7	mA
						V _{DD} = 2.0 V	1.2	1.7	mA
		HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input	3.0	4.6	mA	
					Resonator connection	3.2	4.8	mA	
				Normal operation	Square wave input	3.0	4.6	mA	
					Resonator connection	3.2	4.8	mA	
			f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input	1.9	2.7	mA	
					Resonator connection	1.9	2.7	mA	
				Normal operation	Square wave input	1.9	2.7	mA	
					Resonator connection	1.9	2.7	mA	
		LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input	1.1	1.7	mA	
					Resonator connection	1.1	1.7	mA	
			Normal operation	Square wave input	1.1	1.7	mA		
				Resonator connection	1.1	1.7	mA		
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C	Normal operation	Square wave input	4.1		μA	
					Resonator connection	4.2		μA	
				Normal operation	Square wave input	4.1	4.9	μA	
					Resonator connection	4.2	5.0	μA	
				Normal operation	Square wave input	4.2	5.5	μA	
					Resonator connection	4.3	5.6	μA	
f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C	Normal operation		Square wave input	4.2	6.3	μA			
			Resonator connection	4.3	6.4	μA			
	Normal operation		Square wave input	4.2	6.3	μA			
			Resonator connection	4.3	6.4	μA			
	Normal operation		Square wave input	4.8	7.7	μA			
			Resonator connection	4.9	7.8	μA			
f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C	Normal operation	Square wave input	4.8	7.7	μA				
		Resonator connection	4.9	7.8	μA				

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation).
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(1) Flash ROM: 16 to 64 KB of 20- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V		0.54	1.63	mA	
					V _{DD} = 3.0 V		0.54	1.63	mA	
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V		0.44	1.28	mA	
					V _{DD} = 3.0 V		0.44	1.28	mA	
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V		0.40	1.00	mA	
					V _{DD} = 3.0 V		0.40	1.00	mA	
				LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V		260	530	μA
					V _{DD} = 2.0 V		260	530	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V		420	640	μA	
					V _{DD} = 2.0 V		420	640	μA	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.28	1.00	mA	
					Resonator connection		0.45	1.17	mA	
					f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		0.28	1.00	mA
					Resonator connection		0.45	1.17	mA	
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input		0.19	0.60	mA	
					Resonator connection		0.26	0.67	mA	
		f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V		Square wave input		0.19	0.60	mA		
				Resonator connection		0.26	0.67	mA		
		LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input		95	330	μA		
				Resonator connection		145	380	μA		
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input		95	330	μA		
				Resonator connection		145	380	μA		
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} , T _A = -40°C	Square wave input		0.25		μA		
				Resonator connection		0.44		μA		
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +25°C	Square wave input		0.30	0.57	μA		
				Resonator connection		0.49	0.76	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +50°C	Square wave input		0.33	1.17	μA		
				Resonator connection		0.52	1.36	μA		
			f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +70°C	Square wave input		0.36	1.97	μA		
				Resonator connection		0.55	2.16	μA		
		f _{SUB} = 32.768 kHz ^{Note 5} , T _A = +85°C	Square wave input		0.97	3.37	μA			
		Resonator connection		1.16	3.56	μA				
IDD3 Note 6	STOP mode Note 8	T _A = -40°C			0.18		μA			
		T _A = +25°C			0.23	0.50	μA			
		T _A = +50°C			0.26	1.10	μA			
		T _A = +70°C			0.29	1.90	μA			
		T _A = +85°C			0.90	3.30	μA			

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} and EV_{DD0} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When operating real-time clock (RTC) and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} < 2.4\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

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- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current	I _{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V	2.3		mA	
						V _{DD} = 3.0 V		2.3		mA
				Normal operation	V _{DD} = 5.0 V		5.2	8.5	mA	
					V _{DD} = 3.0 V		5.2	8.5	mA	
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		4.1	6.6	mA
						V _{DD} = 3.0 V		4.1	6.6	mA
			f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.0	4.7	mA	
					V _{DD} = 3.0 V		3.0	4.7	mA	
			LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.3	2.1	mA
						V _{DD} = 2.0 V		1.3	2.1	mA
			LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.3	1.8	mA
						V _{DD} = 2.0 V		1.3	1.8	mA
		HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	5.5	mA	
					Resonator connection		3.6	5.7	mA	
			f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	5.5	mA	
					Resonator connection		3.6	5.7	mA	
			f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.2	mA	
					Resonator connection		2.1	3.2	mA	
			f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.2	mA	
					Resonator connection		2.1	3.2	mA	
		LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.0	mA	
					Resonator connection		1.2	2.0	mA	
			f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.0	mA	
					Resonator connection		1.2	2.0	mA	
Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C	Normal operation	Square wave input		4.8		μA			
			Resonator connection		4.9		μA			
	f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C	Normal operation	Square wave input		4.9	5.9	μA			
			Resonator connection		5.0	6.0	μA			
	f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C	Normal operation	Square wave input		4.9	7.6	μA			
			Resonator connection		5.0	7.7	μA			
	f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C	Normal operation	Square wave input		5.2	9.3	μA			
			Resonator connection		5.3	9.4	μA			
	f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C	Normal operation	Square wave input		6.1	13.3	μA			
			Resonator connection		6.2	13.4	μA			

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation).
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V	0.62	1.86	mA
					V _{DD} = 3.0 V	0.62	1.86	mA
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V	0.50	1.45	mA
					V _{DD} = 3.0 V	0.50	1.45	mA
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V	0.44	1.11	mA
					V _{DD} = 3.0 V	0.44	1.11	mA
			LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V	290	620	μA
				V _{DD} = 2.0 V	290	620	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V	440	680	μA
					V _{DD} = 2.0 V	440	680	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.31	1.08	mA
					Resonator connection	0.48	1.28	mA
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.31	1.08	mA
					Resonator connection	0.48	1.28	mA
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.21	0.63	mA
					Resonator connection	0.28	0.71	mA
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.21	0.63	mA
					Resonator connection	0.28	0.71	mA
		LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	110	360	μA	
				Resonator connection	160	420	μA	
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input	110	360	μA	
				Resonator connection	160	420	μA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = -40°C	Square wave input	0.28		μA	
				Resonator connection	0.47		μA	
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input	0.34	0.61	μA	
				Resonator connection	0.53	0.80	μA	
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input	0.37	2.30	μA	
				Resonator connection	0.56	2.49	μA	
f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.61	4.03	μA			
	Resonator connection		0.80	4.22	μA			
f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input	1.55	8.04	μA				
	Resonator connection	1.74	8.23	μA				
I _{DD3} Note 6	STOP mode Note 8	T _A = -40°C		0.19		μA		
		T _A = +25°C		0.25	0.52	μA		
		T _A = +50°C		0.28	2.21	μA		
		T _A = +70°C		0.52	3.94	μA		
		T _A = +85°C		1.46	7.95	μA		

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When operating real-time clock (RTC) and setting ultra-low current consumption ($AMPHS1 = 1$). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

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- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit	
Supply current	I _{DD1} ^{Note 1}	Operating mode	HS (high-speed main) mode ^{Note 5}	f _{IH} = 32 MHz ^{Note 3}	Basic operation	V _{DD} = 5.0 V	2.6		mA	
						V _{DD} = 3.0 V		2.6		mA
				Normal operation	V _{DD} = 5.0 V		6.1	9.5	mA	
					V _{DD} = 3.0 V		6.1	9.5	mA	
				f _{IH} = 24 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		4.8	7.4	mA
						V _{DD} = 3.0 V		4.8	7.4	mA
			f _{IH} = 16 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V		3.5	5.3	mA	
					V _{DD} = 3.0 V		3.5	5.3	mA	
			LS (low-speed main) mode ^{Note 5}	f _{IH} = 8 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.5	2.3	mA
						V _{DD} = 2.0 V		1.5	2.3	mA
			LV (low-voltage main) mode ^{Note 5}	f _{IH} = 4 MHz ^{Note 3}	Normal operation	V _{DD} = 3.0 V		1.5	2.0	mA
						V _{DD} = 2.0 V		1.5	2.0	mA
			HS (high-speed main) mode ^{Note 5}	f _{MX} = 20 MHz ^{Note 2} , V _{DD} = 5.0 V	Normal operation	Square wave input		3.9	6.1	mA
						Resonator connection		4.1	6.3	mA
		Normal operation			Square wave input		3.9	6.1	mA	
					Resonator connection		4.1	6.3	mA	
		f _{MX} = 10 MHz ^{Note 2} , V _{DD} = 3.0 V		Normal operation	Square wave input		2.5	3.7	mA	
					Resonator connection		2.5	3.7	mA	
				Normal operation	Square wave input		2.5	3.7	mA	
					Resonator connection		2.5	3.7	mA	
		LS (low-speed main) mode ^{Note 5}	f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.2	mA	
					Resonator connection		1.4	2.2	mA	
			f _{MX} = 8 MHz ^{Note 2} , V _{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.2	mA	
					Resonator connection		1.4	2.2	mA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 4} T _A = -40°C	Normal operation	Square wave input		5.4		μA	
					Resonator connection		5.5		μA	
			f _{SUB} = 32.768 kHz ^{Note 4} T _A = +25°C	Normal operation	Square wave input		5.5	6.5	μA	
					Resonator connection		5.6	6.6	μA	
f _{SUB} = 32.768 kHz ^{Note 4} T _A = +50°C	Normal operation		Square wave input		5.6	9.4	μA			
			Resonator connection		5.7	9.5	μA			
f _{SUB} = 32.768 kHz ^{Note 4} T _A = +70°C	Normal operation		Square wave input		5.9	12.0	μA			
			Resonator connection		6.0	12.1	μA			
f _{SUB} = 32.768 kHz ^{Note 4} T _A = +85°C	Normal operation		Square wave input		6.8	16.3	μA			
			Resonator connection		6.9	16.4	μA			

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. When high-speed on-chip oscillator and subsystem clock are stopped.
 3. When high-speed system clock and subsystem clock are stopped.
 4. When high-speed on-chip oscillator and high-speed system clock are stopped. When real-time counter and watchdog timer is stopped. When $AMPHS1 = 1$ (Ultra-low power consumption oscillation).
 5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$

- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(3) 128-pin products, and flash ROM: 384 to 512 KB of 44- to 100-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

(2/2)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{IH} = 32 MHz ^{Note 4}	V _{DD} = 5.0 V	0.62	1.89	mA
					V _{DD} = 3.0 V	0.62	1.89	mA
				f _{IH} = 24 MHz ^{Note 4}	V _{DD} = 5.0 V	0.50	1.48	mA
					V _{DD} = 3.0 V	0.50	1.48	mA
				f _{IH} = 16 MHz ^{Note 4}	V _{DD} = 5.0 V	0.44	1.12	mA
					V _{DD} = 3.0 V	0.44	1.12	mA
			LS (low-speed main) mode Note 7	f _{IH} = 8 MHz ^{Note 4}	V _{DD} = 3.0 V	290	620	μA
				V _{DD} = 2.0 V	290	620	μA	
			LV (low-voltage main) mode Note 7	f _{IH} = 4 MHz ^{Note 4}	V _{DD} = 3.0 V	460	700	μA
					V _{DD} = 2.0 V	460	700	μA
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.31	1.14	mA
					Resonator connection	0.48	1.34	mA
				f _{MX} = 20 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.31	1.14	mA
					Resonator connection	0.48	1.34	mA
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 5.0 V	Square wave input	0.21	0.68	mA
					Resonator connection	0.28	0.76	mA
				f _{MX} = 10 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	0.21	0.68	mA
					Resonator connection	0.28	0.76	mA
		LS (low-speed main) mode Note 7	f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 3.0 V	Square wave input	110	390	μA	
				Resonator connection	160	450	μA	
			f _{MX} = 8 MHz ^{Note 3} , V _{DD} = 2.0 V	Square wave input	110	390	μA	
				Resonator connection	160	450	μA	
		Subsystem clock operation	f _{SUB} = 32.768 kHz ^{Note 5} T _A = -40°C	Square wave input	0.31		μA	
				Resonator connection	0.50		μA	
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +25°C	Square wave input	0.38	0.66	μA	
				Resonator connection	0.57	0.85	μA	
			f _{SUB} = 32.768 kHz ^{Note 5} T _A = +50°C	Square wave input	0.46	3.49	μA	
				Resonator connection	0.65	3.68	μA	
f _{SUB} = 32.768 kHz ^{Note 5} T _A = +70°C	Square wave input		0.75	6.10	μA			
	Resonator connection		0.94	6.29	μA			
f _{SUB} = 32.768 kHz ^{Note 5} T _A = +85°C	Square wave input	1.65	10.46	μA				
	Resonator connection	1.84	10.65	μA				
I _{DD3} Note 6	STOP mode Note 8	T _A = -40°C		0.19		μA		
		T _A = +25°C		0.26	0.54	μA		
		T _A = +50°C		0.34	3.37	μA		
		T _A = +70°C		0.63	5.98	μA		
		T _A = +85°C		1.53	10.34	μA		

(Notes and Remarks are listed on the next page.)

- Notes**
1. Total current flowing into V_{DD} , EV_{DD0} and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} or V_{SS} , EV_{SS0} . The values below the MAX. column include the peripheral operation current (except for background operation (BGO)). However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.
 2. During HALT instruction execution by flash memory.
 3. When high-speed on-chip oscillator and subsystem clock are stopped.
 4. When high-speed system clock and subsystem clock are stopped.
 5. When operating real-time clock (RTC) and setting ultra-low current consumption ($AMPHS1 = 1$). When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 6. When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.
 7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 - HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 16\text{ MHz}$
 - LS (low-speed main) mode: $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 8\text{ MHz}$
 - LV (low-voltage main) mode: $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V} @ 1\text{ MHz to } 4\text{ MHz}$
 8. Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.

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- Remarks**
1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
 2. f_{IH} : High-speed on-chip oscillator clock frequency
 3. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)
 4. Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(4) Common to RL78/G13 all products**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD}0} = \text{EV}_{\text{DD}1} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS}0} = \text{EV}_{\text{SS}1} = 0\text{ V}$)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
RTC operating current	I_{RTC} ^{Notes 1, 2}	$f_{\text{SUB}} = 32.768\text{ kHz}$	Real-time clock operation		0.02		μA
			12-bit Interval timer operation		0.02		μA
Watchdog timer operating current	I_{WDT} ^{Notes 2, 3}	$f_{\text{IL}} = 15\text{ kHz}$			0.22		μA
A/D converter operating current	I_{ADC} ^{Note 4}	When conversion at maximum speed	Normal mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 5.0\text{ V}$		1.3	1.7	mA
			Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$		0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}				75.0		μA
Temperature sensor operating current	I_{TMPS}				75.0		μA
LVD operating current	I_{LVI} ^{Note 5}				0.08		μA
BGO operating current	I_{BGO} ^{Note 6}				2.50	12.20	mA
SNOOZE operating current	I_{SNOZ}	ADC operation	The mode is performed ^{Note 7}		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, $\text{AV}_{\text{REFP}} = \text{V}_{\text{DD}} = 3.0\text{ V}$		1.20	1.44	mA
		CSI/UART operation		0.70	0.84	mA	

Notes 1. Current flowing only to the real-time clock (excluding the operating current of the XT1 oscillator). The value of the current value of the RL78/G13 microcontrollers is the sum of the values of either $I_{\text{DD}1}$ or $I_{\text{DD}2}$, and I_{RTC} , when the real-time clock operates in operation mode or HALT mode. $I_{\text{DD}2}$ subsystem clock operation includes the operational current of the real-time clock.

2. When high speed on-chip oscillator and high-speed system clock are stopped.

<R>

3. Current flowing only to the watchdog timer (including the operating current of the 15-kHz low-speed on-chip oscillator). The current value of the RL78/G13 microcontrollers is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{WDT} when the watchdog timer is in operation.

4. Current flowing only to the A/D converter. The current value of the RL78/G13 microcontrollers is the sum of $I_{\text{DD}1}$ or $I_{\text{DD}2}$ and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

<R>

5. Current flowing only to the LVD circuit. The current value of the RL78/G13 microcontrollers is the sum of $I_{\text{DD}1}$, $I_{\text{DD}2}$ or $I_{\text{DD}3}$ and I_{LVI} .

6. Current flowing only to the BGO. The current value of the RL78/G13 microcontrollers is the sum of $I_{\text{DD}1}$ or $I_{\text{DD}2}$ and I_{BGO} when the BGO operates in an operation mode.

<R>

7. For shift time to the SNOOZE mode, see 18.2.3 SNOOZE mode in the RL78/G13 User's Manual.

Remarks 1. f_{IL} : Low-speed on-chip oscillator clock frequency

2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

3. f_{CLK} : CPU/peripheral hardware clock frequency

4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

2.4 AC Characteristics

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125	1	μs	
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs	
			LV (low-voltage main) mode	1.6 V ≤ V _{DD} ≤ 5.5 V	0.25	1	μs	
			LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.125	1	μs	
			Subsystem clock (f _{SUB}) operation	1.8 V ≤ V _{DD} ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	2.7 V ≤ V _{DD} ≤ 5.5 V	0.03125	1	μs	
				2.4 V ≤ V _{DD} < 2.7 V	0.0625	1	μs	
			LV (low-voltage main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V	0.25	1	μs	
LS (low-speed main) mode	1.8 V ≤ V _{DD} ≤ 5.5 V		0.125	1	μs			
External system clock frequency	f _{ex}	2.7 V ≤ V _{DD} ≤ 5.5 V		1.0		20.0	MHz	
		1.8 V ≤ V _{DD} < 2.7 V		1.0		8.0	MHz	
		1.6 V ≤ V _{DD} < 1.8 V		1.0		4.0	MHz	
	f _{exs}			32		35	kHz	
External system clock input high-level width, low-level width	t _{EXH} , t _{EXL}	2.7 V ≤ V _{DD} ≤ 5.5 V		24			ns	
		1.8 V ≤ V _{DD} < 2.7 V		60			ns	
		1.6 V ≤ V _{DD} < 1.8 V		120			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
T100 to T107, T110 to T117 input high-level width, low-level width	t _{TIH} , t _{TIL}			1/f _{MCK} +10			ns ^{Note}	
TO00 to TO07, TO10 to TO17 output frequency	f _{ro}	HS (high-speed main) mode	4.0 V ≤ EV _{DD0} ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV _{DD0} < 4.0 V			8	MHz	
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
		LV (low-voltage main) mode	1.6 V ≤ EV _{DD0} ≤ 5.5 V			2	MHz	
		LS (low-speed main) mode	1.8 V ≤ EV _{DD0} ≤ 5.5 V			4	MHz	
		1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz		
PCLBUZ0, PCLBUZ1 output frequency	f _{PCL}	HS (high-speed main) mode	4.0 V ≤ EV _{DD0} ≤ 5.5 V			16	MHz	
			2.7 V ≤ EV _{DD0} < 4.0 V			8	MHz	
			1.8 V ≤ EV _{DD0} < 2.7 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
		LV (low-voltage main) mode	1.8 V ≤ EV _{DD0} ≤ 5.5 V			4	MHz	
			1.6 V ≤ EV _{DD0} < 1.8 V			2	MHz	
Interrupt input high-level width, low-level width	t _{INTH} , t _{INTL}	INTP0	1.6 V ≤ V _{DD} ≤ 5.5 V	1			μs	
		INTP1 to INTP11	1.6 V ≤ EV _{DD0} ≤ 5.5 V	1			μs	
Key interrupt input low-level width	t _{KR}	KR0 to KR7	1.8 V ≤ EV _{DD0} ≤ 5.5 V	250			ns	
			1.6 V ≤ EV _{DD0} < 1.8 V	1			μs	
RESET low-level width	t _{RSL}			10			μs	

(Note and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when $E_{VDD0} < V_{DD}$

$1.8\text{ V} \leq E_{VDD0} < 2.7\text{ V}$: MIN. 125 ns

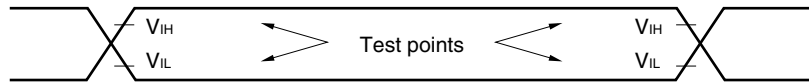
$1.6\text{ V} \leq E_{VDD0} < 1.8\text{ V}$: MIN. 250 ns

Remark f_{MCK} : Timer array unit operation clock frequency

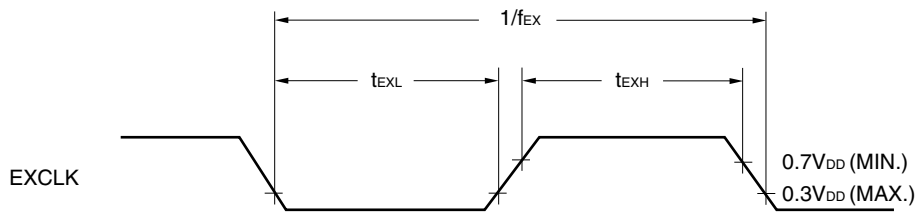
(Operation clock to be set by the CKSmn0, CKSmn1 bits of timer mode register mn (TMRmn).

m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7))

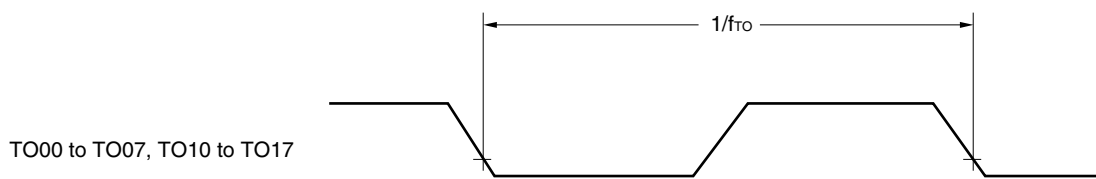
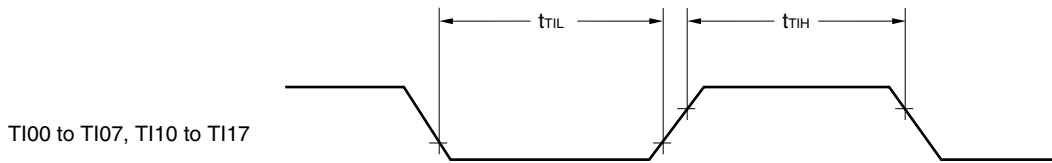
AC Timing Test Points



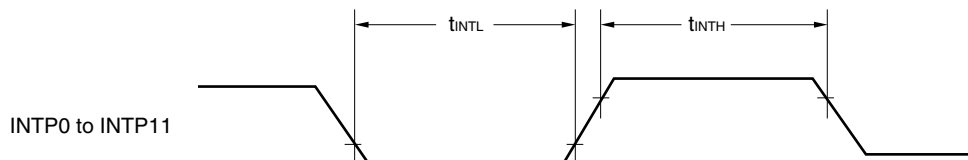
External System Clock Timing



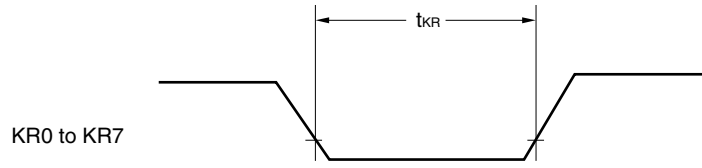
TI/TO Timing



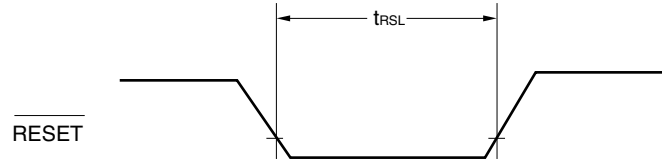
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Peripheral Functions Characteristics

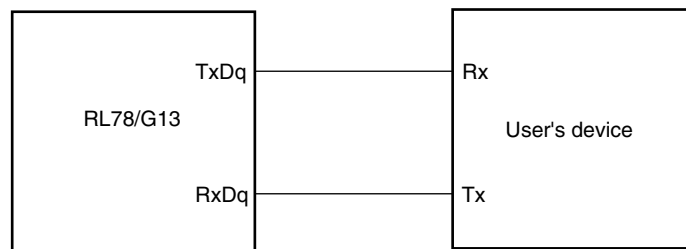
2.5.1 Serial array unit

(1) During communication at same potential (UART mode) (dedicated baud rate generator output)

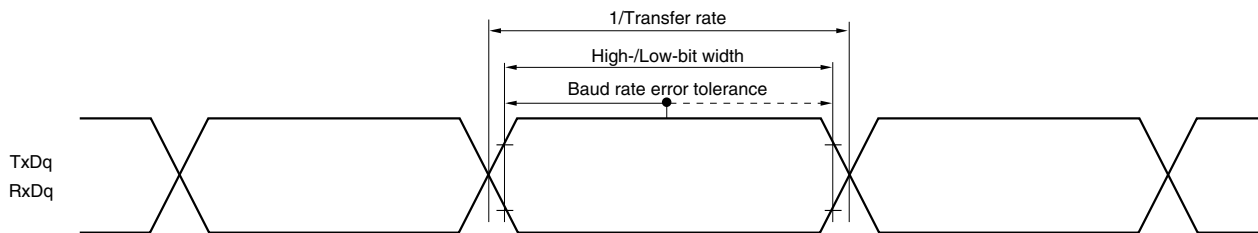
($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate ^{Note 1}					$f_{MCK}/6$ ^{Note 2}	bps
		Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			5.3	Mbps

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Notes 1. Transfer rate in the SNOOZE mode is MAX. 9600 bps, MIN. 4800 bps.

2. The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.

$2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps

$1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps

$1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remarks 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

2. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode ($f_{MCK}/2$), SCKp... internal clock output, coresponding CSI00 only)**($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	62.5 ^{Note 1}			ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 7$			ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{KCY1}/2 - 10$			ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	23			ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	33 ^{Note 5}			ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{KSI1}	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	10			ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO1}	$C = 20\text{ pF}$ ^{Note 6}			10	ns

Notes 1. The value must also be $2/f_{CLK}$ or more.**2.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.**3.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.**4.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.**5.** Using the f_{MCK} within 24 MHz.**6.** C is the load capacitance of the SCKp and SOp output lines.**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).**Remarks 1.** This specification is valid only when CSI00's peripheral I/O redirect function is not used.**2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)**3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode ($f_{MCK}/4$), SCKp... internal clock output)
($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{CY1}	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	125 ^{Note 1}			ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	250 ^{Note 1}			ns
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	500 ^{Note 1}			ns
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	1000 ^{Note 1}			ns
SCKp high-/low-level width	t_{KH1} , t_{KL1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{CY1}/2 - 12$			ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{CY1}/2 - 18$			ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{CY1}/2 - 38$			ns
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{CY1}/2 - 50$			ns
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	$t_{CY1}/2 - 100$			ns
Slp setup time (to SCKp \uparrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	44			ns
		$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	44			ns
		$2.4\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	75			ns
		$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	110			ns
		$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$	220			ns
Slp hold time (from SCKp \uparrow) ^{Note 3}	t_{KSH1}		19			ns
Delay time from SCKp \downarrow to SOp output ^{Note 4}	t_{KSO1}	$C = 30\text{ pF}$ ^{Note 5}			25	ns

Notes 1. The value must also be $4/f_{CLK}$ or more.

- When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.
- C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks** 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)
- f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)**($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EV}_{\text{DD0}} = \text{EV}_{\text{DD1}} \leq \text{V}_{\text{DD}} \leq 5.5\text{ V}$, $\text{V}_{\text{SS}} = \text{EV}_{\text{SS0}} = \text{EV}_{\text{SS1}} = 0\text{ V}$)**

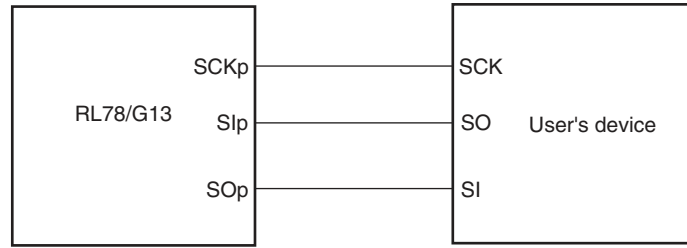
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
SCKp cycle time ^{Note 5}	t_{KCY2}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{\text{MCK}}$	$8/f_{\text{MCK}}$		ns	
			$f_{\text{MCK}} \leq 20\text{ MHz}$	$6/f_{\text{MCK}}$		ns	
		$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$8/f_{\text{MCK}}$		ns	
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$6/f_{\text{MCK}}$		ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	$8/f_{\text{MCK}}$		ns	
			$f_{\text{MCK}} \leq 16\text{ MHz}$	$6/f_{\text{MCK}}$		ns	
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$	$6/f_{\text{MCK}}$		ns		
SCKp high-/low-level width	t_{KH2} , t_{KL2}	$1.6\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$t_{\text{KCY2}}/2$			ns	
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$1/f_{\text{MCK}}+20$			ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$1/f_{\text{MCK}}+30$			ns	
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$	$1/f_{\text{MCK}}+40$			ns	
Slp hold time (from SCKp \uparrow) ^{Note 2}	t_{KSI2}	$2.7\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$	$1/f_{\text{MCK}}+31$			ns	
		$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$	$1/f_{\text{MCK}}+31$			ns	
		$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$	$1/f_{\text{MCK}}+250$			ns	
Delay time from SCKp \downarrow to SOp output ^{Note 3}	t_{KSO2}	$C = 30\text{ pF}$ ^{Note 4}	$4.0\text{ V} \leq \text{EV}_{\text{DD0}} \leq 5.5\text{ V}$			$2/f_{\text{MCK}}+44$	ns
			$2.7\text{ V} \leq \text{EV}_{\text{DD0}} < 4.0\text{ V}$			$2/f_{\text{MCK}}+44$	ns
			$2.4\text{ V} \leq \text{EV}_{\text{DD0}} < 2.7\text{ V}$			$2/f_{\text{MCK}}+75$	ns
			$1.8\text{ V} \leq \text{EV}_{\text{DD0}} < 2.4\text{ V}$			$2/f_{\text{MCK}}+110$	ns
			$1.6\text{ V} \leq \text{EV}_{\text{DD0}} < 1.8\text{ V}$			$2/f_{\text{MCK}}+220$	ns

- Notes**
- When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp setup time becomes “to SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 - When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The Slp hold time becomes “from SCKp \downarrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 - When $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 0$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAP}_{\text{mn}} = 0$ and $\text{CKP}_{\text{mn}} = 1$, or $\text{DAP}_{\text{mn}} = 1$ and $\text{CKP}_{\text{mn}} = 0$.
 - C is the load capacitance of the SOp output lines.
 - Transfer rate in the SNOOZE mode : MAX. 1 Mbps

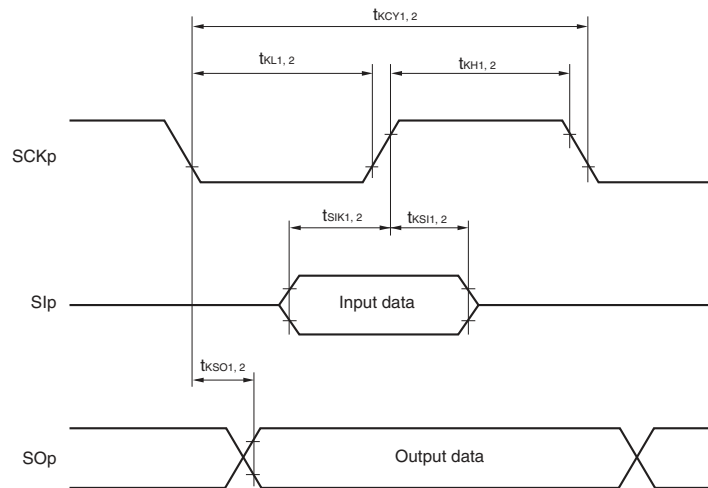
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
- p : CSI number ($p = 00, 01, 10, 11, 20, 21, 30, 31$), m : Unit number ($m = 0, 1$),
 n : Channel number ($n = 0$ to 3), g : PIM number ($g = 0, 1, 4, 5, 8, 14$)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m : Unit number,
 n : Channel number ($\text{mn} = 00$ to $03, 10$ to 13))

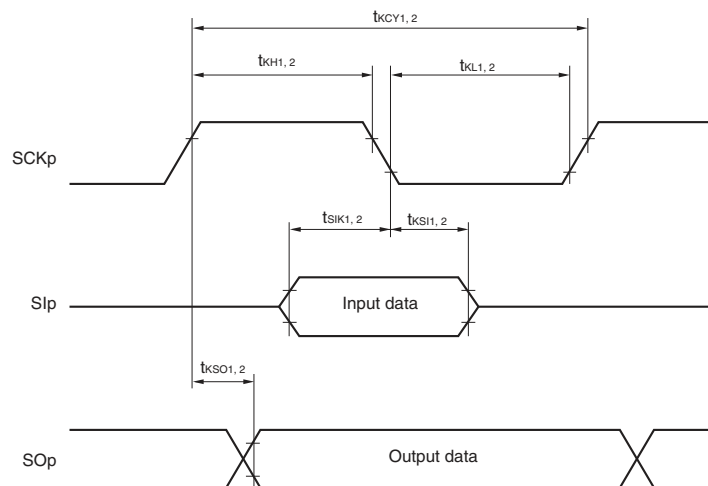
CSI mode connection diagram (during communication at same potential)



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



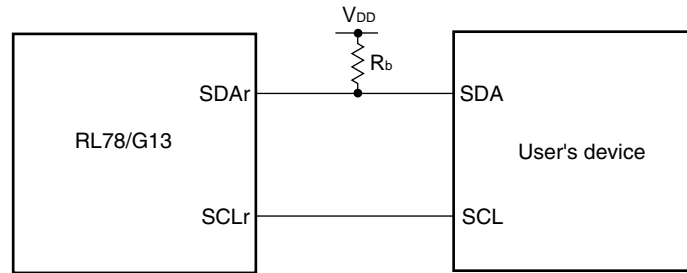
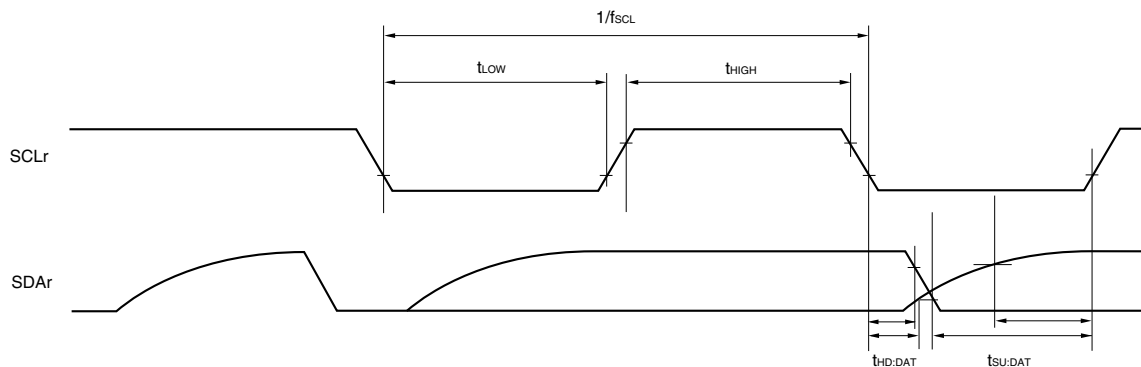
- Remarks**
1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) During communication at same potential (simplified I²C mode)(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ		1000	kHz
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ		400	kHz
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ		300	kHz
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ		250	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1150		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1550		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1850		ns
Data setup time (reception)	t _{SU:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 <small>Note</small>		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 <small>Note</small>		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 <small>Note</small>		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 <small>Note</small>		ns
Data hold time (transmission)	t _{HD:DAT}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	ns

Note Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

(**Caution** and **Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)Simplified I²C mode serial transfer timing (during communication at same potential)

Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance
 - r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14),
h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

**(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
(dedicated baud rate generator output) (1/2)**

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		Reception	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$,			$f_{MCK}/6$ ^{Note 1}	bps
			$2.7\text{ V} \leq V_b \leq 4.0\text{ V}$	Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			5.3
			$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$,			$f_{MCK}/6$ ^{Note 1}	bps
			$2.3\text{ V} \leq V_b \leq 2.7\text{ V}$	Theoretical value of the maximum transfer rate $f_{CLK} = 32\text{ MHz}$, $f_{MCK} = f_{CLK}$			5.3
			$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$,			$f_{MCK}/6$ Notes 1 to 3	bps
			$1.6\text{ V} \leq V_b \leq 2.0\text{ V}$	Theoretical value of the maximum transfer rate $f_{CLK} = 8\text{ MHz}$, $f_{MCK} = f_{CLK}$			1.3

- Notes**
- Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps
 - Use it with $EV_{DD0} \geq V_b$.
 - The following conditions are required for low voltage interface when $EV_{DD0} < V_{DD}$.
 $2.4\text{ V} \leq EV_{DD0} < 2.7\text{ V}$: MAX. 2.6 Mbps
 $1.8\text{ V} \leq EV_{DD0} < 2.4\text{ V}$: MAX. 1.3 Mbps
 $1.6\text{ V} \leq EV_{DD0} < 1.8\text{ V}$: MAX. 0.6 Mbps

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
- $V_b[V]$: Communication line voltage
 - q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
 - UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)
(dedicated baud rate generator output) (2/2)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Transfer rate		Transmission	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V			Notes 1, 2	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 1.4 kΩ, V _b = 2.7 V			2.8 ^{Note 3}	Mbps
			2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V			Notes 2, 4	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 2.7 kΩ, V _b = 2.3 V			1.2 ^{Note 5}	Mbps
			1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V			Notes 2, 6, 7	bps
			Theoretical value of the maximum transfer rate C _b = 50 pF, R _b = 5.5 kΩ, V _b = 1.6 V			0.43 ^{Note 8}	Mbps

Notes 1. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EV_{DD0} ≤ 5.5 V and 2.7 V ≤ V_b ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 2. Transfer rate in the SNOOZE mode : MAX. 9600 bps, MIN. 4800 bps
- 3. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 1 above to calculate the maximum transfer rate under conditions of the customer.
- 4. The smaller maximum transfer rate derived by using f_{MCK}/6 or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EV_{DD0} < 4.0 V and 2.3 V ≤ V_b ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

- 5. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 4 above to calculate the maximum transfer rate under conditions of the customer.

Notes 6. Use it with $EV_{DD0} \geq V_b$.

7. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

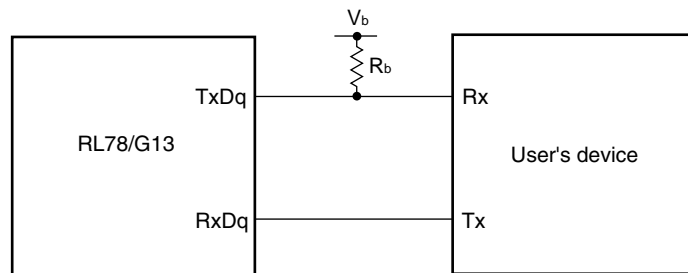
* This value is the theoretical value of the relative difference between the transmission and reception sides.

8. This value as an example is calculated when the conditions described in the “Conditions” column are met. Refer to Note 7 above to calculate the maximum transfer rate under conditions of the customer.

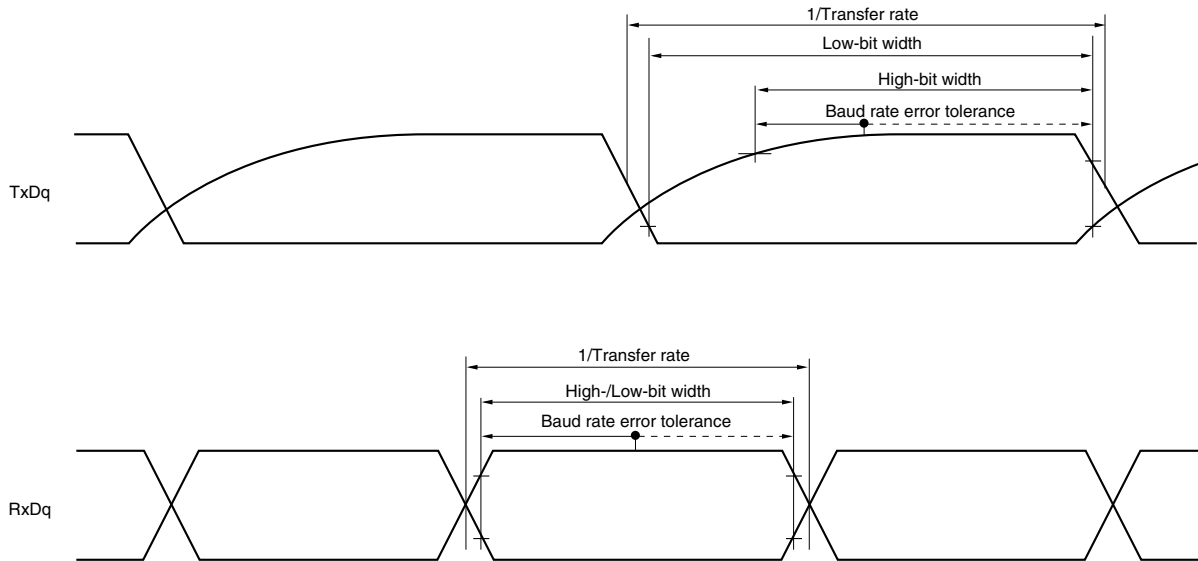
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks 1.** $R_b[\Omega]$:Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
- 4.** UART2 cannot communicate at different potential when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

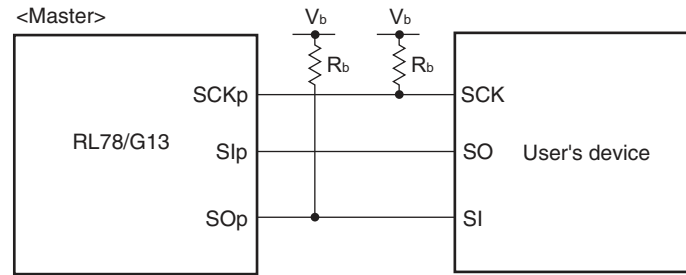
- Remarks**
1. UART2 cannot communicate at different potentials when bit 1 (PIOR1) of peripheral I/O redirection register (PIOR) is 1.
 2. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage
 3. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

(7) Communication at different potential (2.5 V, 3 V) ($f_{MCK}/2$) (CSI mode) (master mode, SCKp... internal clock output, coresponding CSI00 only)(T_A = -40 to +85°C, 2.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t _{KCY1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	200 ^{Note 1}			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	300 ^{Note 1}			ns
SCKp high-level width	t _{KH1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 50			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 120			ns
SCKp low-level width	t _{KL1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	t _{KCY1} /2 - 7			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	t _{KCY1} /2 - 10			ns
Slp setup time (to SCKp↑) ^{Note 2}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	58			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	121			ns
Slp hold time (from SCKp↑) ^{Note 2}	t _{SI1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10			ns
Delay time from SCKp↓ to SOp output ^{Note 2}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			60	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			130	ns
Slp setup time (to SCKp↓) ^{Note 3}	t _{SIK1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	21			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	29			ns
Slp hold time (from SCKp↓) ^{Note 3}	t _{SI1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ	10			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ	10			ns
Delay time from SCKp↑ to SOp output ^{Note 3}	t _{KSO1}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 20 pF, R _b = 1.4 kΩ			10	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 20 pF, R _b = 2.7 kΩ			10	ns

(Note, Caution and Remark are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



- Notes**
1. The value must also be $2/f_{CLK}$ or more.
 2. When $DAPmn = 0$ and $CKPmn = 0$, or $DAPmn = 1$ and $CKPmn = 1$.
 3. When $DAPmn = 0$ and $CKPmn = 1$, or $DAPmn = 1$ and $CKPmn = 0$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number ($p = 00$), m: Unit number ($m = 0$), n: Channel number ($n = 0$),
g: PIM and POM number ($g = 1$)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number ($mn = 00$))
 4. This specification is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) ($f_{MCK}/4$) (CSI mode) (master mode, SCKp... internal clock output) (1/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	300 ^{Note}			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	500 ^{Note}			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	1150 ^{Note}			ns
SCKp high-level width	t_{KH1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 75$			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 170$			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 458$			ns
SCKp low-level width	t_{KL1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	$t_{KCY1}/2 - 12$			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	$t_{KCY1}/2 - 18$			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	$t_{KCY1}/2 - 50$			ns

Note The value must also be $4/f_{CLK}$ or more.

Cautions 1. Select the TTL input buffer for the SIp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

2. Use it with $EV_{DD0} \geq V_b$.

Remarks 1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[\text{F}]$: Communication line (SCKp, SOp) load capacitance, $V_b[\text{V}]$: Communication line voltage

2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

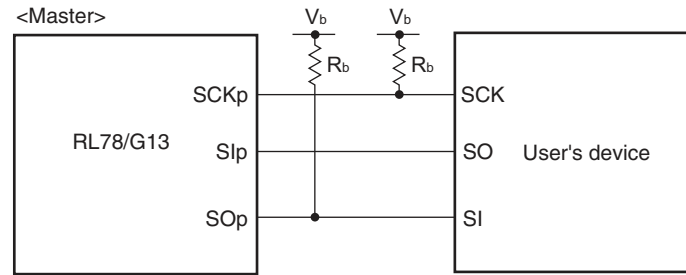
3. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) ($f_{MCK}/4$) (CSI mode) (master mode, SCKp... internal clock output) (2/2)**($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Slp setup time (to SCKp \uparrow) ^{Note 1}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	81			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	177			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	479			ns
Slp hold time (from SCKp \uparrow) ^{Note 1}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	19			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	19			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	19			ns
Delay time from SCKp \downarrow to SOp output ^{Note 1}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			100	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			195	ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			483	ns
Slp setup time (to SCKp \downarrow) ^{Note 2}	t_{SIK1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	44			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	44			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	110			ns
Slp hold time (from SCKp \downarrow) ^{Note 2}	t_{KSI1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$	19			ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$	19			ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$	19			ns
Delay time from SCKp \uparrow to SOp output ^{Note 2}	t_{KSO1}	$4.0\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$			25	ns
		$2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$			25	ns
		$1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$			25	ns

(Notes, Cautions and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

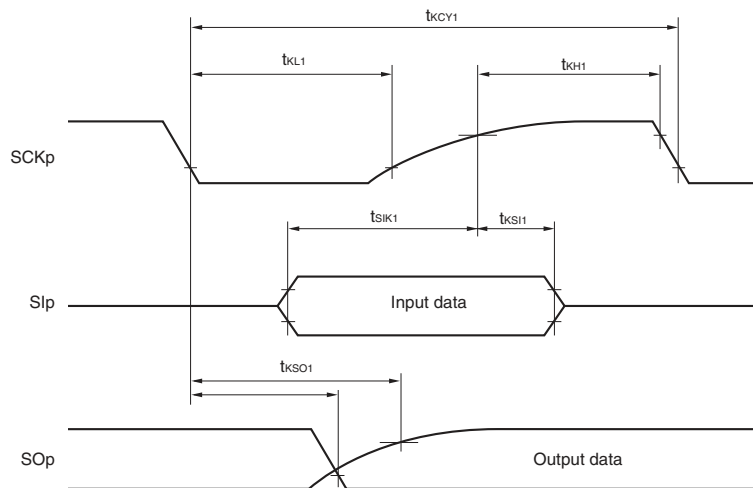


- Notes**
1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

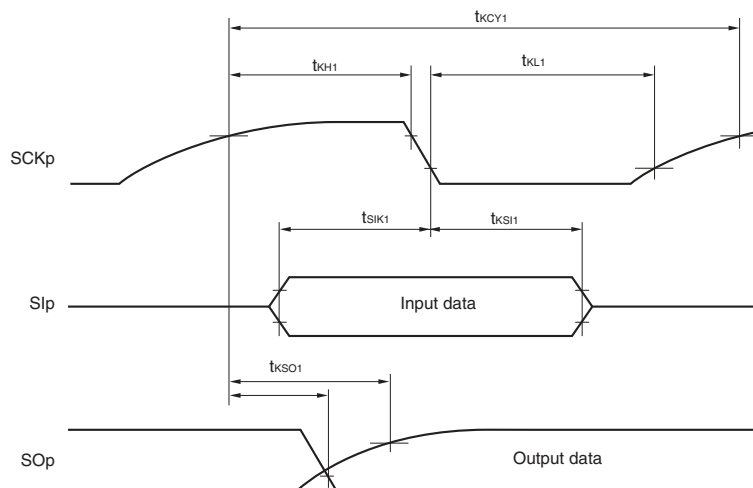
- Cautions**
1. Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).
 2. Use it with $EV_{DD0} \geq V_b$.

- Remarks**
1. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 00, 01, 02, 10, 12, 13), n: Channel number (n = 0, 2), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

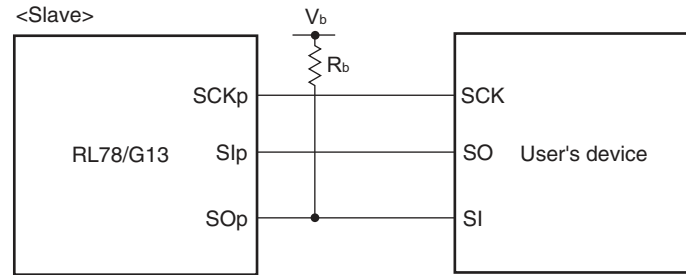
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)

(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
SCKp cycle time ^{Note 1}	t _{KCY2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	24 MHz < f _{MCK}	14/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	12/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 20 MHz	10/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		ns
			f _{MCK} ≤ 4 MHz	6/f _{MCK}		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	24 MHz < f _{MCK}	20/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	16/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	14/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	12/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	8/f _{MCK}		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	24 MHz < f _{MCK}	48/f _{MCK}		ns
			20 MHz < f _{MCK} ≤ 24 MHz	36/f _{MCK}		ns
			16 MHz < f _{MCK} ≤ 20 MHz	32/f _{MCK}		ns
			8 MHz < f _{MCK} ≤ 16 MHz	26/f _{MCK}		ns
			4 MHz < f _{MCK} ≤ 8 MHz	16/f _{MCK}		ns
SCKp high-/low-level width	t _{KH2} , t _{KL2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V	t _{KCY2} /2 – 12			ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V	t _{KCY2} /2 – 18			ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	t _{KCY2} /2 – 50			ns
Slp setup time (to SCKp↑) ^{Note 3}	t _{SIK2}	2.7 V ≤ EV _{DD0} ≤ 5.5 V, 2.3 V ≤ V _b ≤ 4.0 V ^{Note 2}	1/f _{MCK} + 20			ns
		1.8 V ≤ EV _{DD0} ≤ 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2}	1/f _{MCK} + 30			ns
Slp hold time (from SCKp↑) ^{Note 4}	t _{KSI2}		1/f _{MCK} + 31			ns
Delay time from SCKp↓ to SOp output ^{Note 5}	t _{KSO2}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 30 pF, R _b = 1.4 kΩ			2/f _{MCK} + 120	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 30 pF, R _b = 2.7 kΩ			2/f _{MCK} + 214	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 30 pF, R _b = 5.5 kΩ			2/f _{MCK} + 573	ns

(Notes, Caution and Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

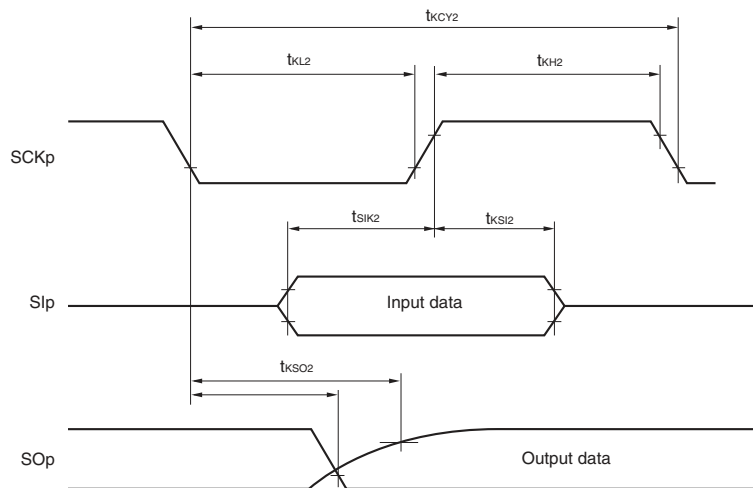


- Notes**
1. Transfer rate in the SNOOZE mode : MAX. 1 Mbps
 2. Use it with $EV_{DD0} \geq V_b$.
 3. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to $SCKp\downarrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 4. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp hold time becomes “from $SCKp\downarrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
 5. When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from $SCKp\uparrow$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.

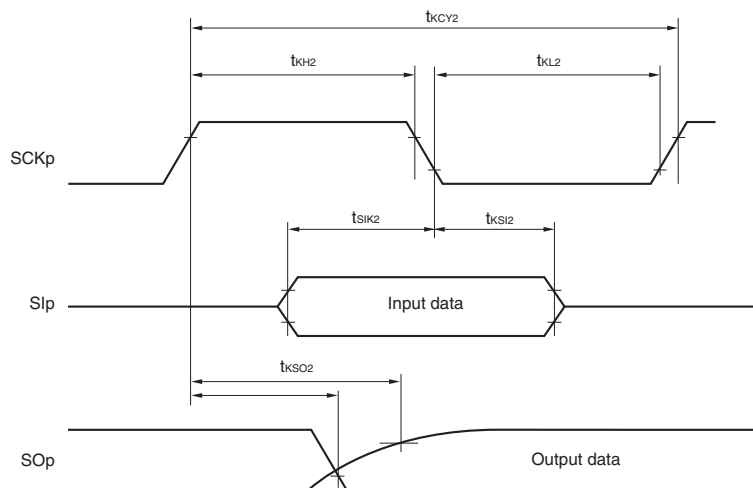
Caution Select the TTL input buffer for the Slp pin and $SCKp$ pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
 2. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
 4. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Caution Select the TTL input buffer for the Slp pin and SCKp pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number,
n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential.
Use other CSI for communication at different potential.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (1/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 1} , C _b = 100 pF, R _b = 5.5 kΩ		300	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 1} , C _b = 100 pF, R _b = 5.5 kΩ	1550		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 1} , C _b = 100 pF, R _b = 5.5 kΩ	610		ns

(Notes, Caution and Remarks are listed on the next page.)

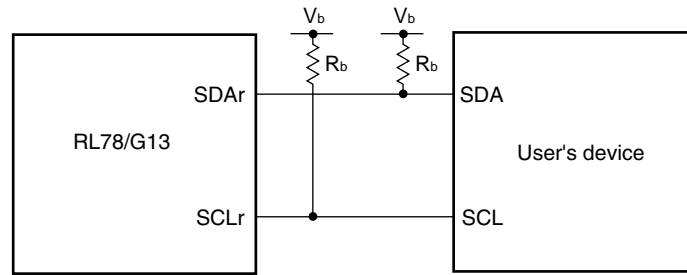
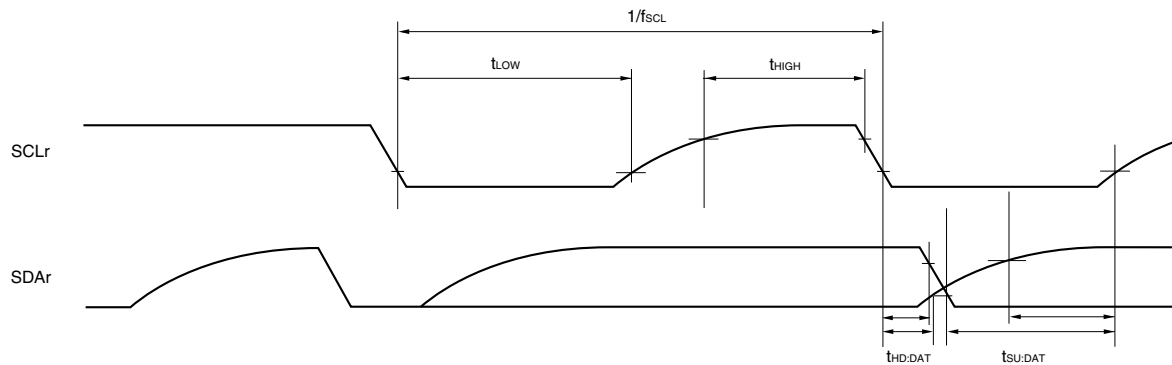
(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode) (2/2)**(T_A = -40 to +85°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)**

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 <small>Note 2</small>		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 <small>Note 2</small>		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 <small>Note 2</small>		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 <small>Note 2</small>		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{<small>Notes 1</small>} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 <small>Note 2</small>		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b < 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{<small>Note 1</small>} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	ns

Notes 1. Use it with EV_{DD0} ≥ V_b.**2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(Remarks is listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)Simplified I²C mode serial transfer timing (during communication at different potential)

Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (When 20- to 52-pin products)/ EV_{DD} tolerance (When 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg).

- Remarks**
- $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
 - r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM, POM number (g = 0, 1, 4, 5, 8, 14)
 - f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))

2.5.2 Serial interface IICA

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

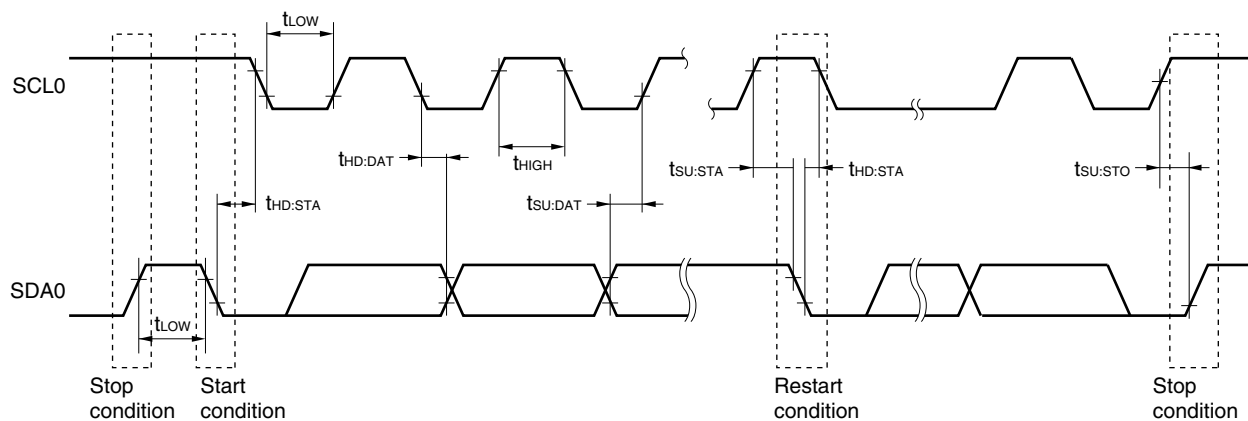
Parameter	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Plus		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCLA0 clock frequency	f_{SCL}	Fast mode plus: $f_{CLK} \geq 10\text{ MHz}$	$2.7\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$					0	1000	kHz
		Fast mode: $f_{CLK} \geq 3.5\text{ MHz}$	$1.8\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$				0	400		kHz
		Normal mode: $f_{CLK} \geq 1\text{ MHz}$	$1.6\text{ V} \leq EV_{DD0} \leq 5.5\text{ V}$		0	100				kHz
Setup time of restart condition	$t_{SU:STA}$		4.7		0.6		0.26		μs	
Hold time ^{Note 1}	$t_{HD:STA}$		4.0		0.6		0.26		μs	
Hold time when SCLA0 = "L"	t_{LOW}		4.7		1.3		0.5		μs	
Hold time when SCLA0 = "H"	t_{HIGH}		4.0		0.6		0.26		μs	
Data setup time (reception)	$t_{SU:DAT}$		250		100		50		ns	
Data hold time (transmission) ^{Note 2}	$t_{HD:DAT}$		0	3.45	0	0.9	0	0.45	μs	
Setup time of stop condition	$t_{SU:STO}$		4.0		0.6		0.26		μs	
Bus-free time	t_{BUF}		4.7		1.3		0.5		μs	

- Notes**
- The first clock pulse is generated after this period when the start/restart condition is detected.
 - The maximum value (MAX.) of $t_{HD:DAT}$ is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: $C_b = 400\text{ pF}$, $R_b = 2.7\text{ k}\Omega$
 Fast mode: $C_b = 320\text{ pF}$, $R_b = 1.1\text{ k}\Omega$
 Fast mode plus: $C_b = 120\text{ pF}$, $R_b = 1.1\text{ k}\Omega$

IICA serial transfer timing



2.5.3 On-chip debug (UART)

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate			115.2 k		1 M	bps

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(1) When $AV_{REF(+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), $AV_{REF(-)} = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI2 to ANI14

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

<R>

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Resolution	RES		8		10	bit		
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 3.5	LSB	
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB	
Conversion time	t_{CONV}	10-bit resolution $AV_{REFP} = V_{DD}$	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs	
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs	
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		57		95	μs
Zero-scale error ^{Notes 1, 2}	E _{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	%FSR	
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.50	%FSR	
Full-scale error ^{Notes 1, 2}	E _{FS}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.25	%FSR	
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.50	%FSR	
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB	
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 5.0	LSB	
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.5	LSB	
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB	
Reference voltage (+)	AV_{REFP}		1.6		V_{DD}	V		
Analog input voltage	V_{AIN}		0		AV_{REFP}	V		
	V_{BGR}	Select interanal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.5	V		

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(2) When $AV_{REF(+)} = AV_{REFP}/ANI0$ ($ADREFP1 = 0, ADREFP0 = 1$), $AV_{REF(-)} = AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = AV_{REFM})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error ^{Note 1}	AINL	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 8.5	LSB
Conversion time	t_{CONV}	10-bit resolution $AV_{REFP} = V_{DD}$	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.35	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 3.5	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 6.0	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution $AV_{REFP} = V_{DD}$	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Reference voltage (+)	AV_{REFP}		1.6		V_{DD}	V	
Analog input voltage	V_{AIN}		0		AV_{REFP} and EV_{DD0}	V	
	V_{BGR}	Select internal reference voltage output $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.5	V	

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(3) When $AV_{REF(+)} = V_{DD}$ (ADREFP1 = 0, ADREFP0 = 0), $AV_{REF(-)} = V_{SS}$ (ADREFM = 0), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error ^{Note 1}	AINL	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 10.5	LSB
Conversion time	t_{CONV}	10-bit resolution	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.85	%FSR
Full-scale error ^{Notes 1, 2}	E_{FS}	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.85	%FSR
Integral linearity error ^{Note 1}	ILE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 6.5	LSB
Differential linearity error ^{Note 1}	DLE	10-bit resolution	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Analog input voltage	V_{AIN}	ANI0 to ANI14		0		V_{DD}	V
		ANI16 to ANI26		0		EV_{DD0}	V
	V_{BGR}	Select interanal reference voltage output, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode	1.38	1.45	1.5		V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

(4) When $AV_{REF (+)}$ = Internal reference voltage ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF (-)}$ = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin : ANI0 to ANI14, ANI16 to ANI26

($T_A = -40$ to $+85^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = V_{BGR} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t_{CONV}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error ^{Notes 1, 2}	E_{ZS}	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	%FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Notes 1. Excludes quantization error ($\pm 1/2$ LSB).

2. This value is indicated as a ratio (%FSR) to the full-scale value.

2.6.2 Temperature sensor characteristics

(T_A = -40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	V _{TMPS25}	Setting ADS register = 80H, T _A = +25°C		1.05		V
Internal reference voltage	V _{CONST}	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	F _{VTMPS}	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	t _{AMP}				5	μs

2.6.3 POR circuit characteristics

(T_A = -40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{POR}	Power supply rise time	1.48	1.51	1.54	V
	V _{PDR}	Power supply fall time	1.47	1.50	1.53	V
Minimum pulse width	T _{PW}		300			μs
Detection delay time					350	μs

2.6.4 LVD circuit characteristics

LVD Detection Voltage of Reset Mode and Interrupt Mode(T_A = -40 to +85°C, V_{PDR} ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection voltage	V _{LVD0}	Power supply rise time	3.98	4.06	4.14	V
		Power supply fall time	3.90	3.98	4.06	V
	V _{LVD1}	Power supply rise time	3.68	3.75	3.82	V
		Power supply fall time	3.60	3.67	3.74	V
	V _{LVD2}	Power supply rise time	3.07	3.13	3.19	V
		Power supply fall time	3.00	3.06	3.12	V
	V _{LVD3}	Power supply rise time	2.96	3.02	3.08	V
		Power supply fall time	2.90	2.96	3.02	V
	V _{LVD4}	Power supply rise time	2.86	2.92	2.97	V
		Power supply fall time	2.80	2.86	2.91	V
	V _{LVD5}	Power supply rise time	2.76	2.81	2.87	V
		Power supply fall time	2.70	2.75	2.81	V
	V _{LVD6}	Power supply rise time	2.66	2.71	2.76	V
		Power supply fall time	2.60	2.65	2.70	V
	V _{LVD7}	Power supply rise time	2.56	2.61	2.66	V
		Power supply fall time	2.50	2.55	2.60	V
	V _{LVD8}	Power supply rise time	2.45	2.50	2.55	V
		Power supply fall time	2.40	2.45	2.50	V
	V _{LVD9}	Power supply rise time	2.05	2.09	2.13	V
		Power supply fall time	2.00	2.04	2.08	V
	V _{LVD10}	Power supply rise time	1.94	1.98	2.02	V
		Power supply fall time	1.90	1.94	1.98	V
	V _{LVD11}	Power supply rise time	1.84	1.88	1.91	V
		Power supply fall time	1.80	1.84	1.87	V
	V _{LVD12}	Power supply rise time	1.74	1.77	1.81	V
		Power supply fall time	1.70	1.73	1.77	V
V _{LVD13}	Power supply rise time	1.64	1.67	1.70	V	
	Power supply fall time	1.60	1.63	1.66	V	
Minimum pulse width	t _{LW}		300			μs
Detection delay time					300	μs

LVD Detection Voltage of Interrupt & Reset Mode**($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5$ V, $V_{SS} = EV_{SS0} = EV_{SS1} = 0$ V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Interrupt and reset mode	V_{LVD13}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 0$, falling reset voltage: 1.6 V	1.60	1.63	1.66	V	
	V_{LVD12}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	V_{LVD11}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	V_{LVD4}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	V_{LVD11}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 0, 1$, falling reset voltage: 1.8 V	1.80	1.84	1.87	V	
	V_{LVD10}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	V_{LVD9}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
	V_{LVD2}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.07	3.13	3.19	V
			Falling interrupt voltage	3.00	3.06	3.12	V
	V_{LVD8}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 0$, falling reset voltage: 2.4 V	2.40	2.45	2.50	V	
	V_{LVD7}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.56	2.61	2.66	V
			Falling interrupt voltage	2.50	2.55	2.60	V
	V_{LVD6}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.66	2.71	2.76	V
			Falling interrupt voltage	2.60	2.65	2.70	V
	V_{LVD1}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.68	3.75	3.82	V
Falling interrupt voltage			3.60	3.67	3.74	V	
V_{LVD5}	$V_{POC2}, V_{POC1}, V_{POC0} = 0, 1, 1$, falling reset voltage: 2.7 V	2.70	2.75	2.81	V		
V_{LVD4}	LVIS1, LVIS0 = 1, 0 (+0.1 V)	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
V_{LVD3}	LVIS1, LVIS0 = 0, 1 (+0.2 V)	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	
V_{LVD0}	LVIS1, LVIS0 = 0, 0 (+1.2 V)	Rising release reset voltage	3.98	4.06	4.14	V	
		Falling interrupt voltage	3.90	3.98	4.06	V	

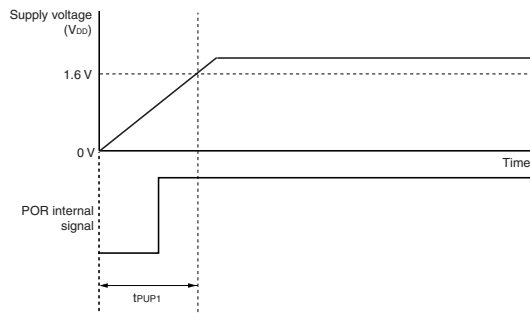
Supply Voltage Rise Time ($T_A = -40$ to $+85^\circ\text{C}$, $V_{SS} = 0$ V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Maximum time to rise to 1.6 V (V_{DD} (MIN.)) ^{Note} (V_{DD} : 0 V \rightarrow 1.6 V)	t_{PUP1}	When RESET input is not used			3.2	ms

Note Make sure to raise the power supply in a shorter time than this.

Supply Voltage Rise Time Timing

- When RESET pin input is not used

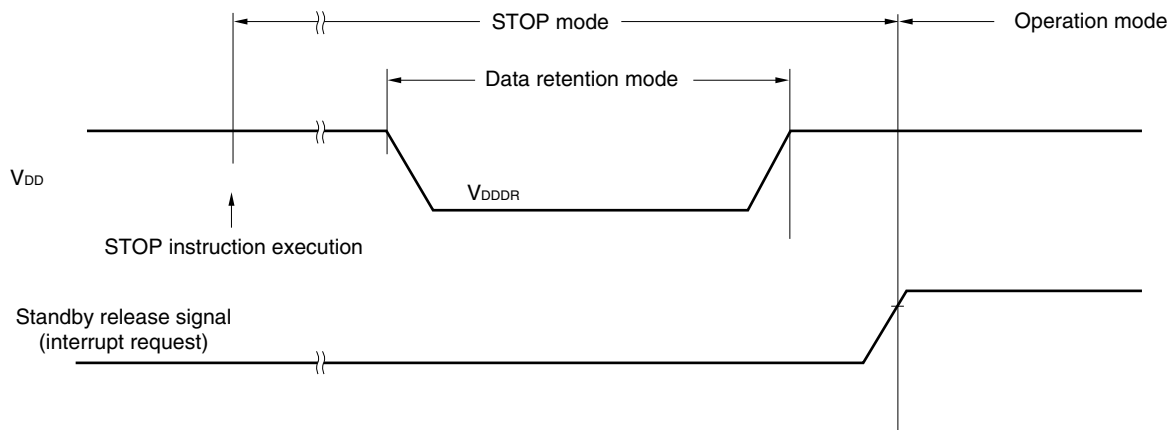


2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics

($T_A = -40$ to $+85^\circ\text{C}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.47 ^{Note}		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.8\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	f_{CLK}	$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1		32	MHz
<R> Number of code flash rewrites <small>Notes 1, 2, 3</small>	C_{erwr}	Retained for 20 years	$T_A = 85^\circ\text{C}$ ^{Note 3}	1,000			Times
<R> Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 years	$T_A = 25^\circ\text{C}$ ^{Note 3}		1,000,000		
		Retained for 5 years	$T_A = 85^\circ\text{C}$ ^{Note 3}	100,000			
		Retained for 20 years	$T_A = 85^\circ\text{C}$ ^{Note 3}	10,000			

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.

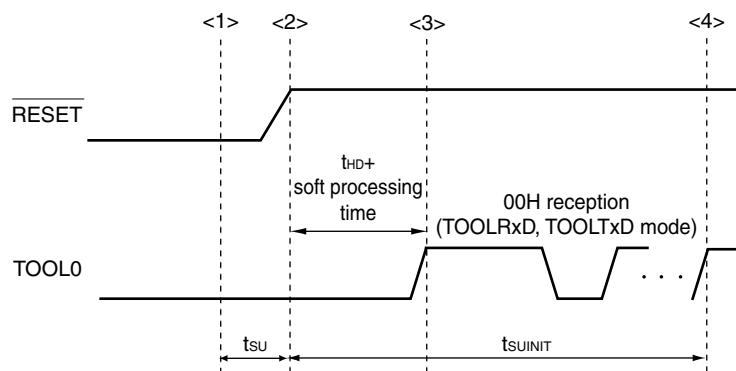
The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer and Renesas Electronics self programming library

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas.

2.9 Timing Specs for Switching Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when a pin reset ends until the initial communication settings are specified	$t_{SUIINIT}$	POR and LVD reset must end before the pin reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until a pin reset ends	t_{SU}	POR and LVD reset must end before the pin reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after a reset ends (except soft processing time)	t_{HD}	POR and LVD reset must end before the pin reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The pins reset ends (POR and LVD reset must end before the pin reset ends.).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark $t_{SUIINIT}$: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.

t_{SU} : How long from when the TOOL0 pin is placed at the low level until a pin reset ends (MIN. 10 μs)

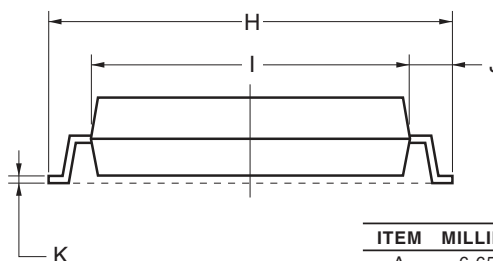
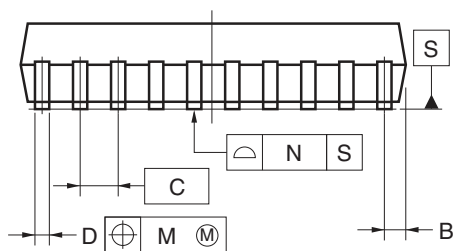
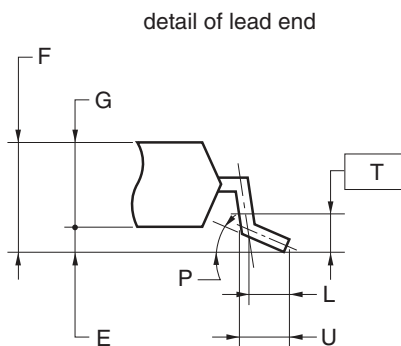
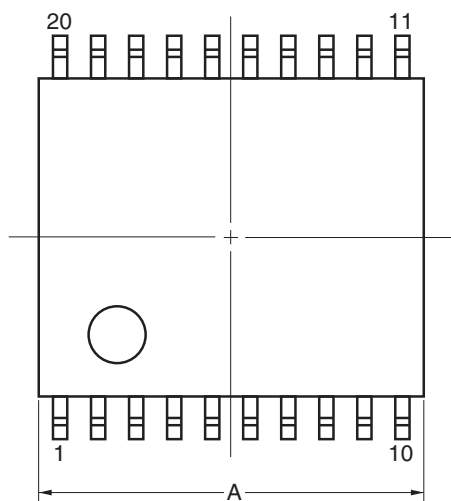
t_{HD} : How long to keep the TOOL0 pin at the low level from when the external and internal resets end (except soft processing time)

3. PACKAGE DRAWINGS

3.1 20-pin products

R5F1006AASP, R5F1006CASP, R5F1006DASP, R5F1006EASP
 R5F1016AASP, R5F1016CASP, R5F1016DASP, R5F1016EASP
 R5F1006ADSP, R5F1006CDSP, R5F1006DDSP, R5F1006EDSP
 R5F1016ADSP, R5F1016CDSP, R5F1016DDSP, R5F1016EDSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP20-0300-0.65	PLSP0020JC-A	S20MC-65-5A4-3	0.12



ITEM	MILLIMETERS
A	6.65±0.15
B	0.475 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

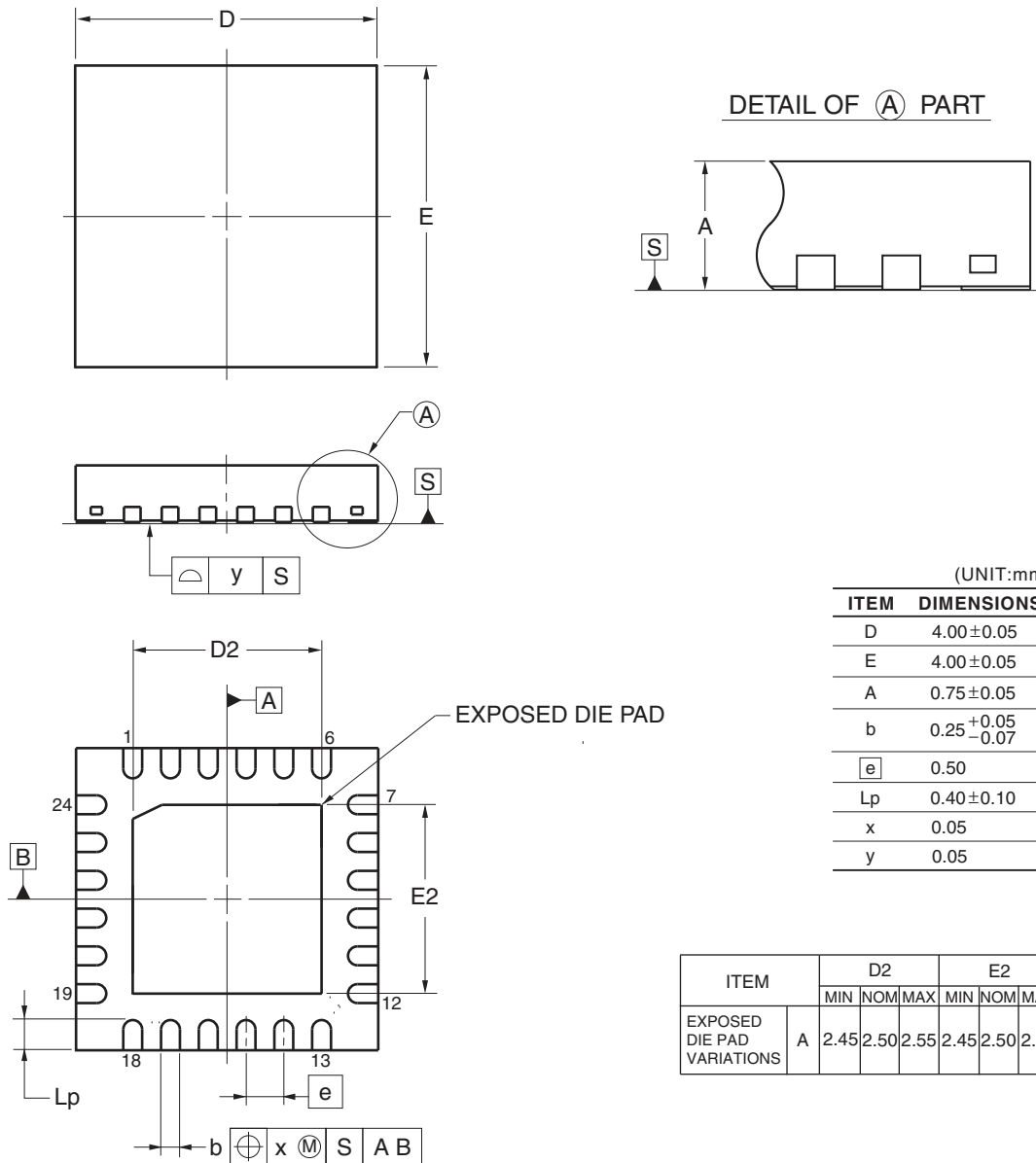
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

3.2 24-pin products

R5F1007AANA, R5F1007CANA, R5F1007DANA, R5F1007EANA
 R5F1017AANA, R5F1017CANA, R5F1017DANA, R5F1017EANA
 R5F1007ADNA, R5F1007CDNA, R5F1007DDNA, R5F1007EDNA
 R5F1017ADNA, R5F1017CDNA, R5F1017DDNA, R5F1017EDNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN24-4x4-0.50	PWQN0024KE-A	P24K8-50-CAB-1	0.04

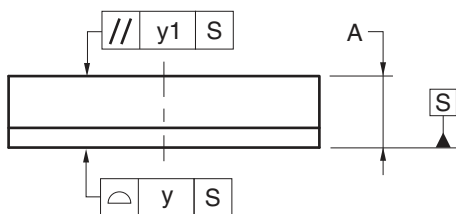
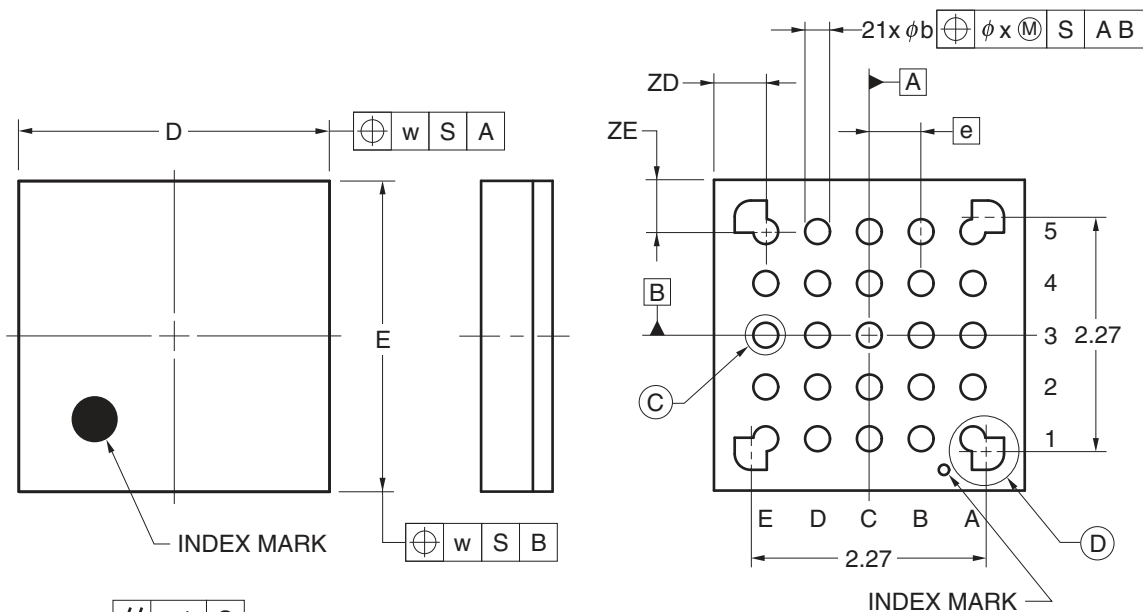


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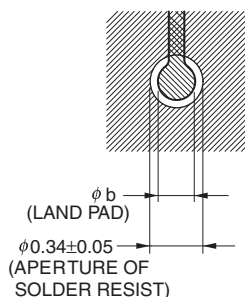
3.3 25-pin products

R5F1008AALA, R5F1008CALA, R5F1008DALA, R5F1008EALA
 R5F1018AALA, R5F1018CALA, R5F1018DALA, R5F1018EALA
 R5F1008ADLA, R5F1008CDLA, R5F1008DDLA, R5F1008EDLA
 R5F1018ADLA, R5F1018CDLA, R5F1018DDLA, R5F1018EDLA

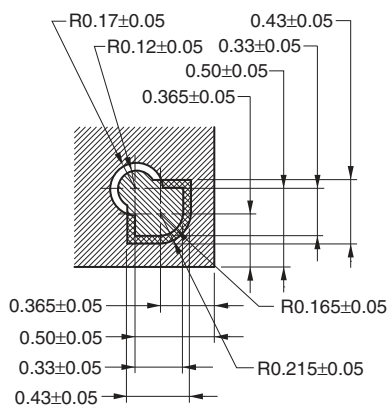
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA25-3x3-0.50	PWLG0025KA-A	P25FC-50-2N2-2	0.01



DETAIL OF (C) PART



DETAIL OF (D) PART



(UNIT:mm)

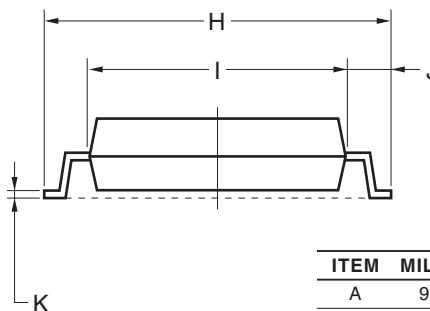
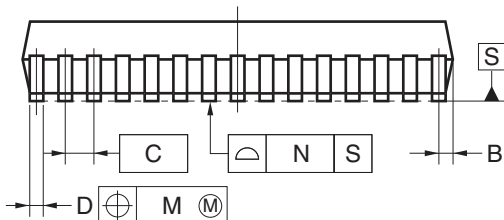
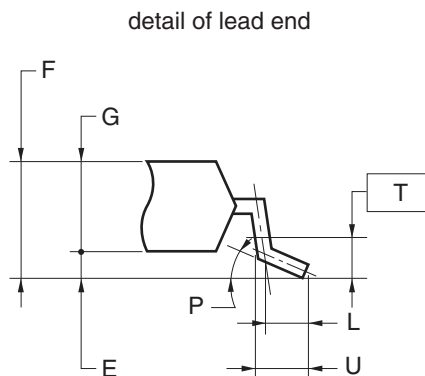
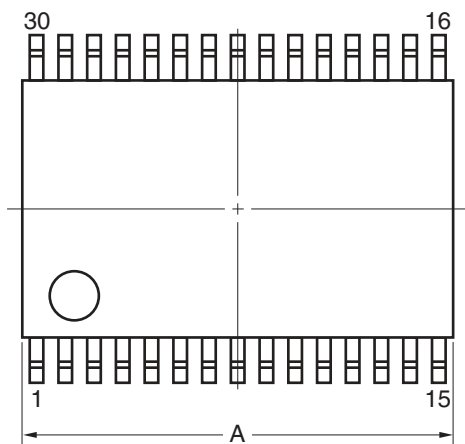
ITEM	DIMENSIONS
D	3.00±0.10
E	3.00±0.10
w	0.20
e	0.50
A	0.69±0.07
b	0.24±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.50
ZE	0.50

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3.4 30-pin products

R5F100AAASP, R5F100ACASP, R5F100ADASP, R5F100AEASP, R5F100AFASP, R5F100AGASP
 R5F101AAASP, R5F101ACASP, R5F101ADASP, R5F101AEASP, R5F101AFASP, R5F101AGASP
 R5F100AADSP, R5F100ACDSP, R5F100ADDSP, R5F100AEDSP, R5F100AFDSP, R5F100AGDSP
 R5F101AADSP, R5F101ACDSP, R5F101ADDSP, R5F101AEDSP, R5F101AFDSP, R5F101AGDSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

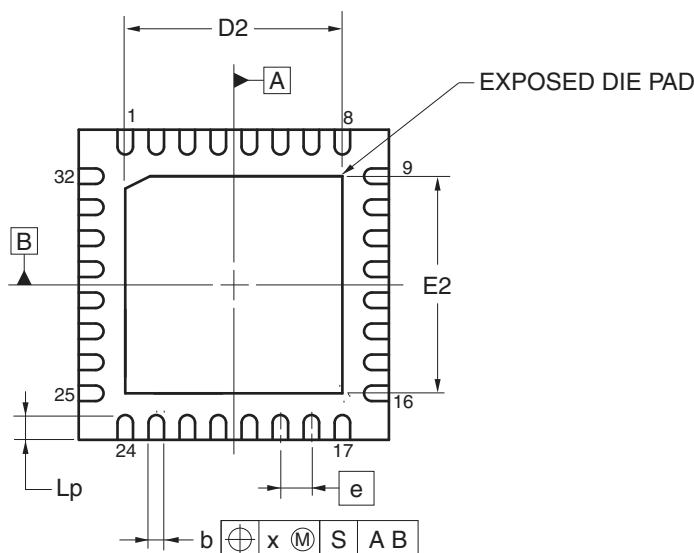
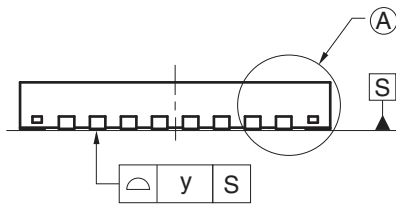
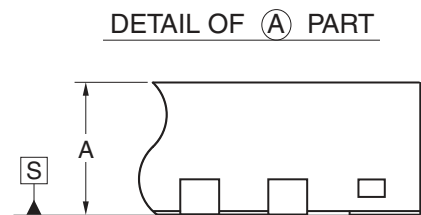
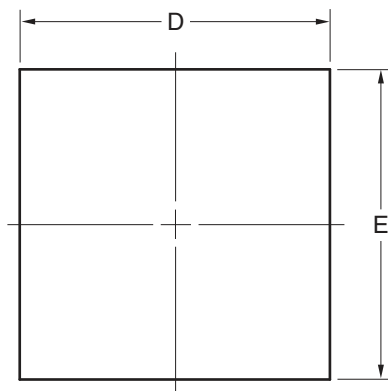
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

3.5 32-pin products

R5F100BAANA, R5F100BCANA, R5F100BDANA, R5F100BEANA, R5F100BFANA, R5F100BGANA
 R5F101BAANA, R5F101BCANA, R5F101BDANA, R5F101BEANA, R5F101BFANA, R5F101BGANA
 R5F100BADNA, R5F100BCDNA, R5F100BDDNA, R5F100BEDNA, R5F100BFDNA, R5F100BGDNA
 R5F101BADNA, R5F101BCDNA, R5F101BDDNA, R5F101BEDNA, R5F101BFDNA, R5F101BGDNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-3	0.06



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.05
E	5.00±0.05
A	0.75±0.05
b	0.25 ^{+0.05} _{-0.07}
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

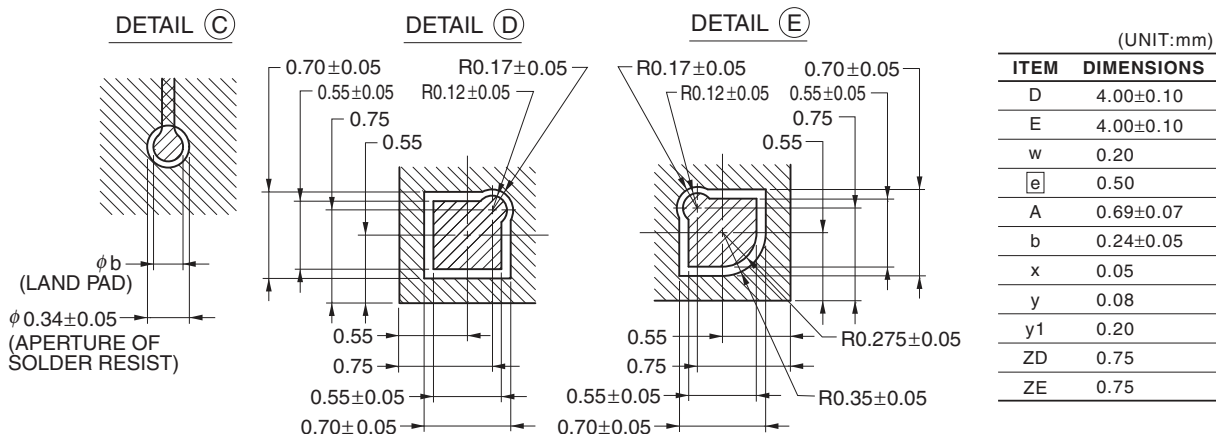
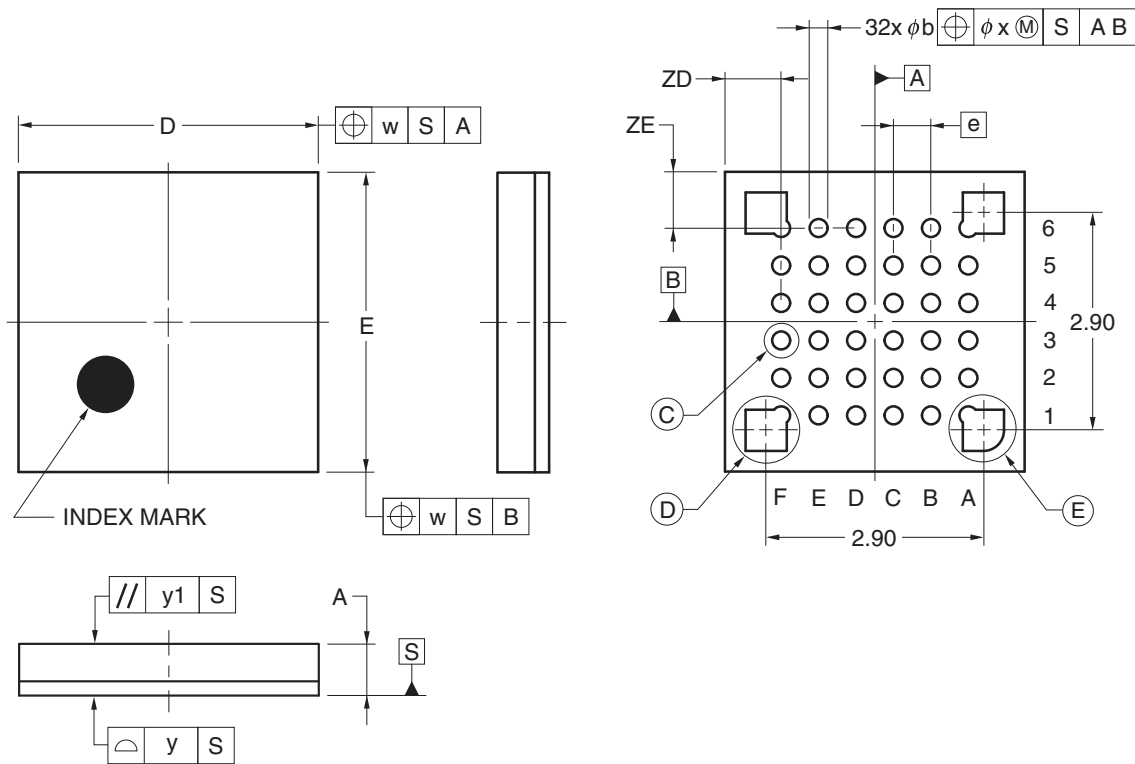
ITEM	A	D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS		3.45	3.50	3.55	3.45	3.50	3.55

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3.6 36-pin products

R5F100CAALA, R5F100CCALA, R5F100CDALA, R5F100CEALA, R5F100CFALA, R5F100CGALA
 R5F101CAALA, R5F101CCALA, R5F101CDALA, R5F101CEALA, R5F101CFALA, R5F101CGALA
 R5F100CADLA, R5F100CCDLA, R5F100CDDL, R5F100CEDLA, R5F100CFDLA, R5F100CGDLA
 R5F101CADLA, R5F101CCDLA, R5F101CDDL, R5F101CEDLA, R5F101CFDLA, R5F101CGDLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

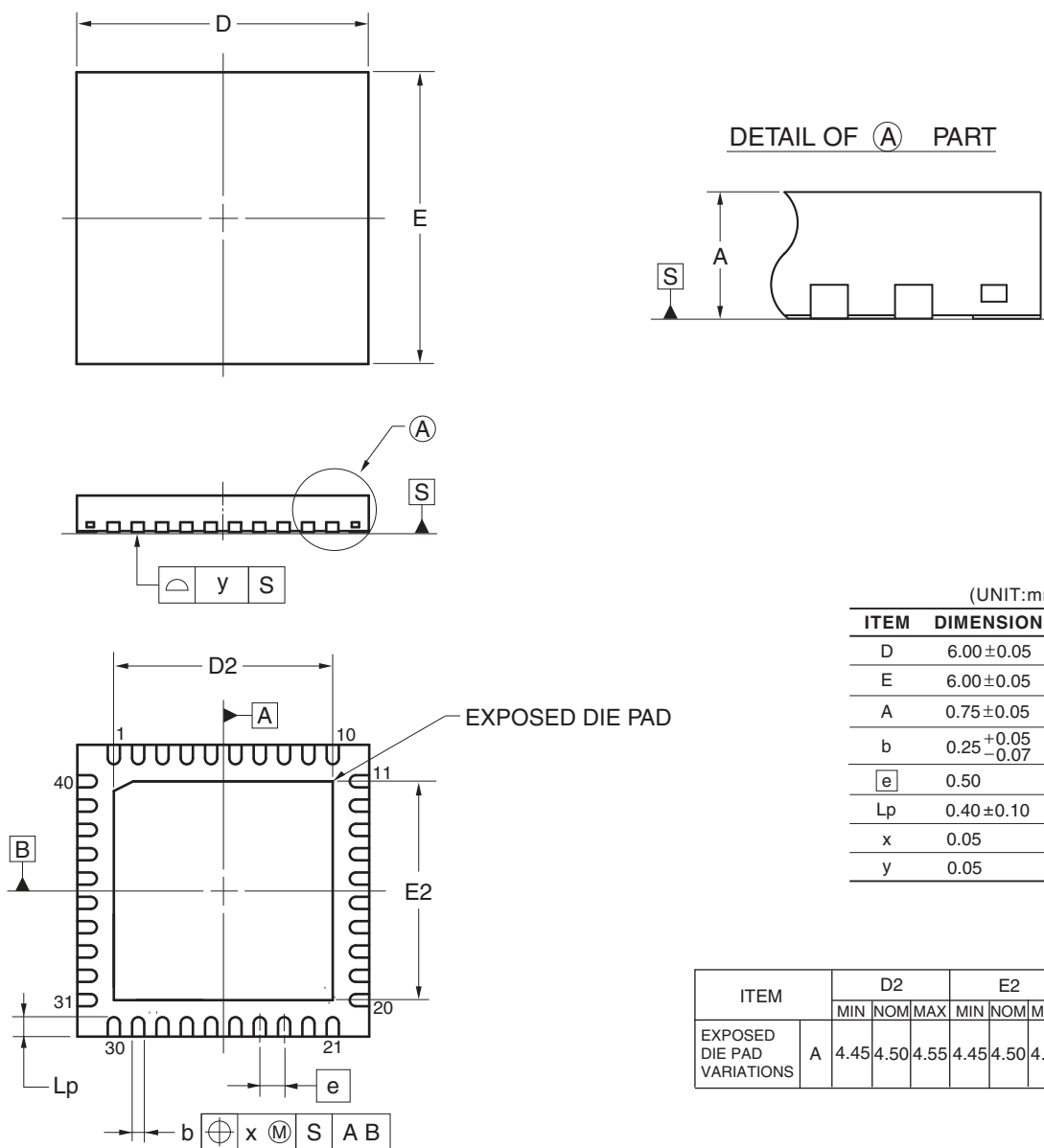


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3.7 40-pin products

R5F100EAANA, R5F100ECANA, R5F100EDANA, R5F100EEANA, R5F100EFANA, R5F100EGANA, R5F100EHANA
 R5F101EAANA, R5F101ECANA, R5F101EDANA, R5F101EEANA, R5F101EFANA, R5F101EGANA, R5F101EHANA
 R5F100EADNA, R5F100ECDNA, R5F100EDDNA, R5F100EEDNA, R5F100EFDNA, R5F100EGDNA, R5F100EHDNA
 R5F101EADNA, R5F101ECDNA, R5F101EDDNA, R5F101EEDNA, R5F101EFDNA, R5F101EGDNA, R5F101EHDNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-3	0.09



(UNIT:mm)

ITEM	DIMENSIONS
D	6.00±0.05
E	6.00±0.05
A	0.75±0.05
b	0.25 ^{+0.05} _{-0.07}
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

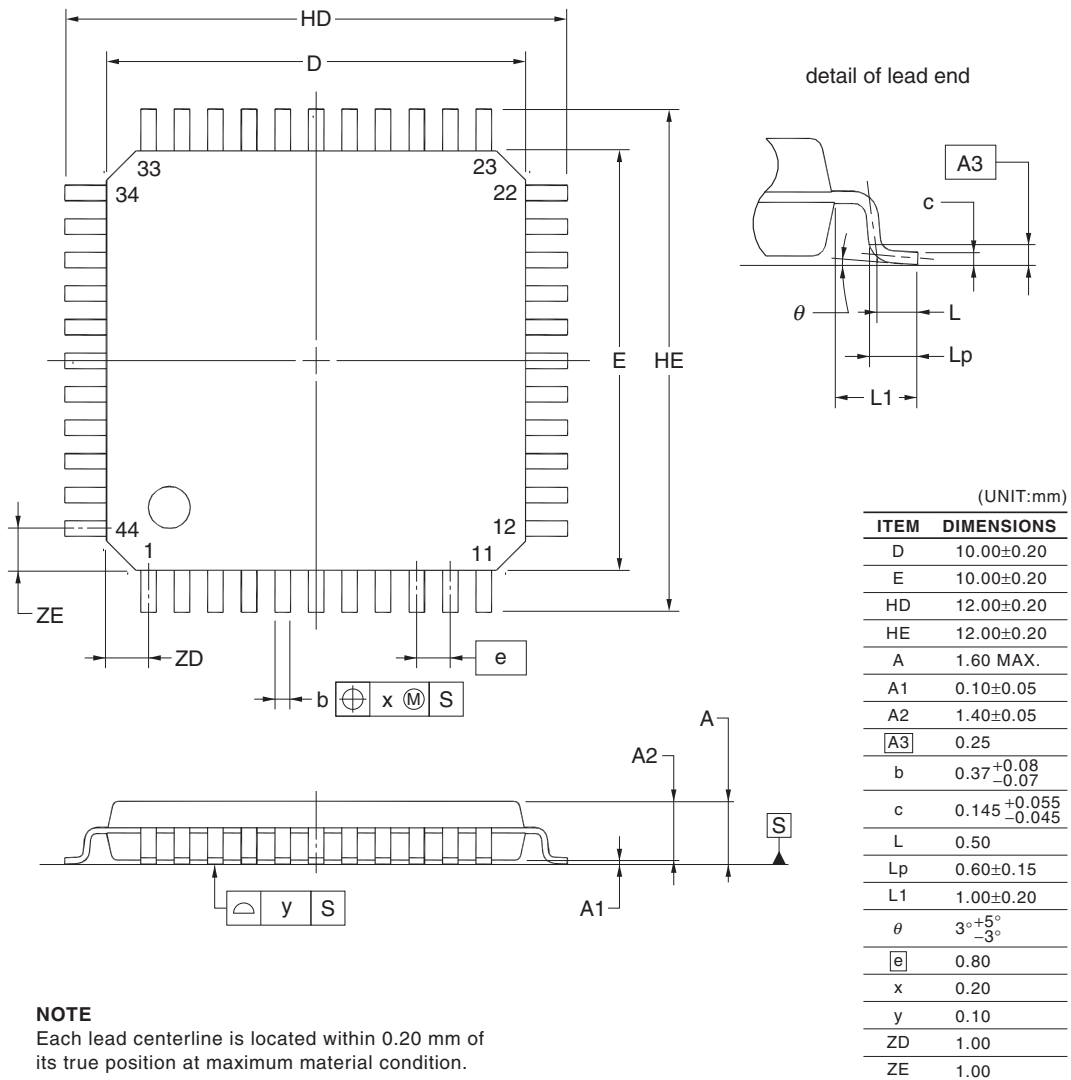
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	4.45	4.50	4.55	4.45	4.50	4.55

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3.8 44-pin products

R5F100FAAFP, R5F100FCAFP, R5F100FDAFP, R5F100FEAFP, R5F100FFAFP, R5F100FGAFP,
 R5F100FHAFP, R5F100FJAFP, R5F100FKAFP, R5F100FLAFP
 R5F101FAAFP, R5F101FCAFP, R5F101FDAFP, R5F101FEAFP, R5F101FFAFP, R5F101FGAFP,
 R5F101FHAFP, R5F101FJAFP, R5F101FKAFP, R5F101FLAFP
 R5F100FADFP, R5F100FCDFP, R5F100FDDFP, R5F100FEDFP, R5F100FFDFP, R5F100FGDFP,
 R5F100FHDFP, R5F100FJDFP, R5F100FKDFP, R5F100FLDFP
 R5F101FADFP, R5F101FCDFP, R5F101FDDFP, R5F101FEDFP, R5F101FFDFP, R5F101FGDFP,
 R5F101FHDFP, R5F101FJDFP, R5F101FKDFP, R5F101FLDFP

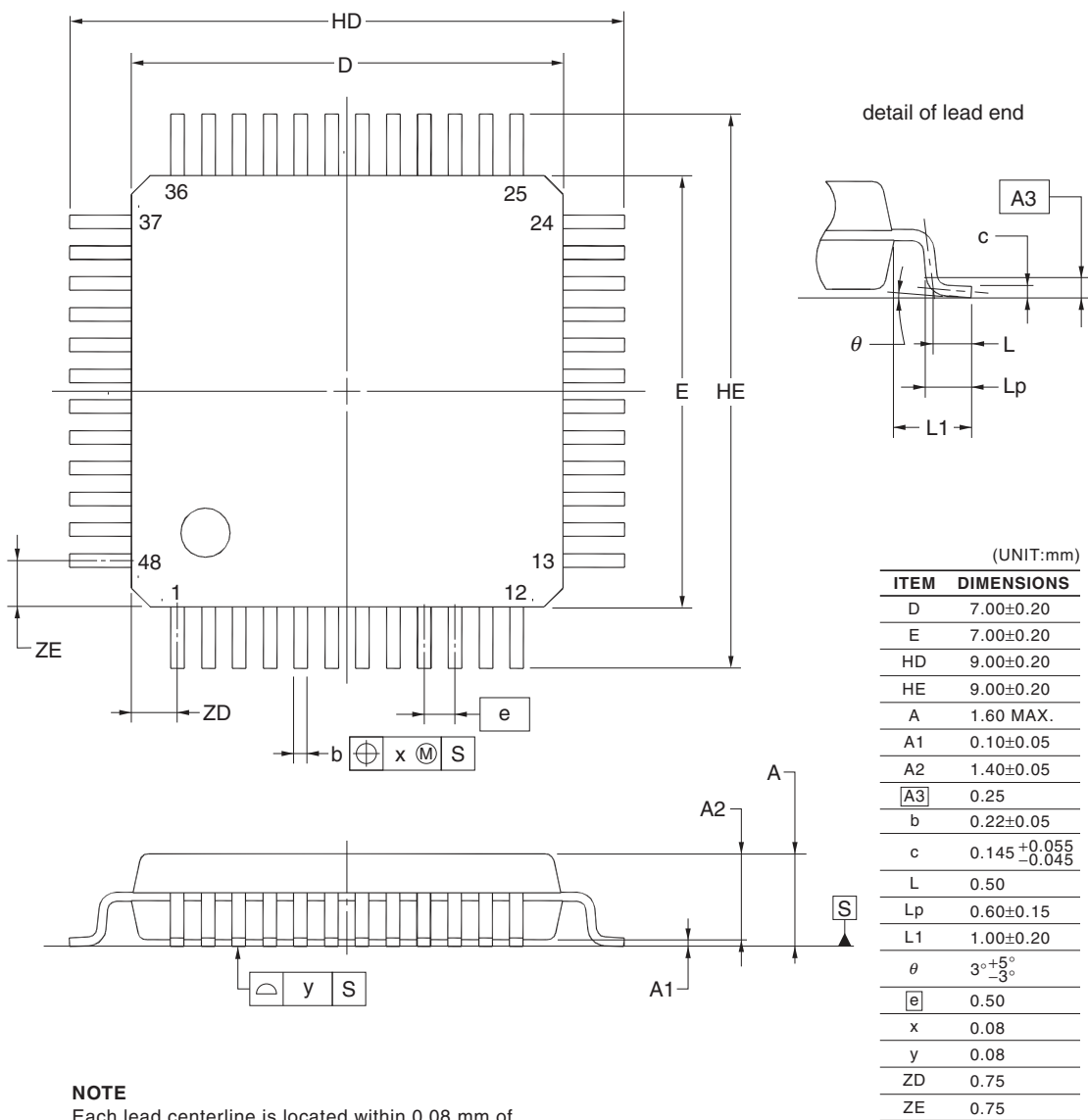
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



3.9 48-pin products

R5F100GAAFB, R5F100GCAFB, R5F100GDADF, R5F100GEAFB, R5F100GFAFB, R5F100GGAFB, R5F100GHAFB, R5F100GJAFB, R5F100GKAFB, R5F100GLAFB
 R5F101GAAFB, R5F101GCAFB, R5F101GDADF, R5F101GEAFB, R5F101GFAFB, R5F101GGAFB, R5F101GHAFB, R5F101GJAFB, R5F101GKAFB, R5F101GLAFB
 R5F100GADFB, R5F100GCDFB, R5F100GDDFB, R5F100GEDFB, R5F100GFDFB, R5F100GGDFB, R5F100GHDFB, R5F100GJDFB, R5F100GKDFB, R5F100GLDFB
 R5F101GADFB, R5F101GCDFB, R5F101GDDFB, R5F101GEDFB, R5F101GFDFB, R5F101GGDFB, R5F101GHDFB, R5F101GJDFB, R5F101GKDFB, R5F101GLDFB

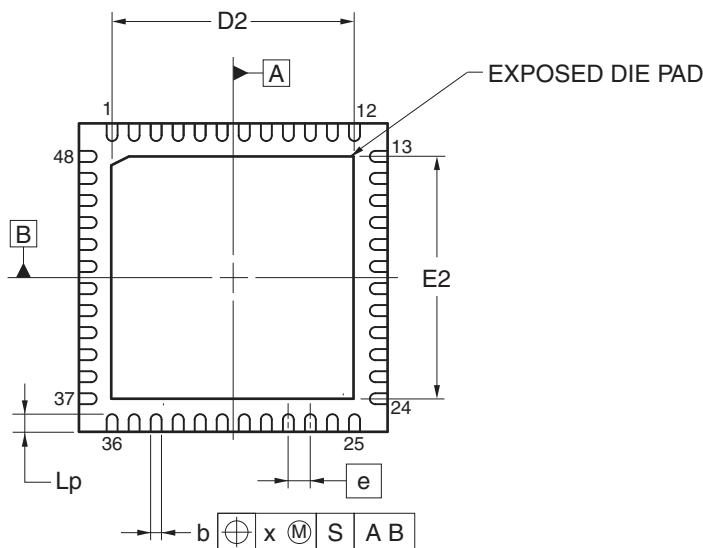
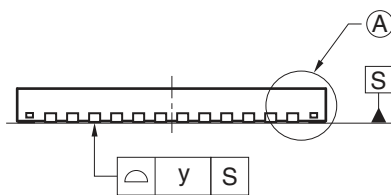
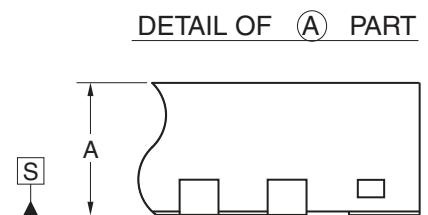
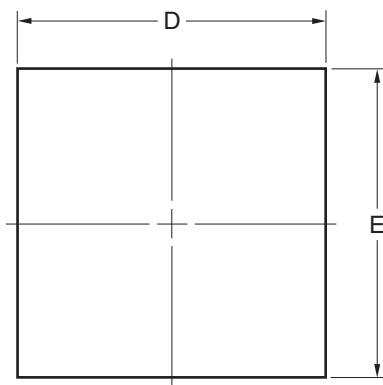
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F100GAANA, R5F100GCANA, R5F100GDANA, R5F100GEANA, R5F100GFANA, R5F100GGANA,
 R5F100GHANA, R5F100GJANA, R5F100GKANA, R5F100GLANA
 R5F101GAANA, R5F101GCANA, R5F101GDANA, R5F101GEANA, R5F101GFANA, R5F101GGANA,
 R5F101GHANA, R5F101GJANA, R5F101GKANA, R5F101GLANA
 R5F100GADNA, R5F100GCDNA, R5F100GDDNA, R5F100GEDNA, R5F100GFDNA, R5F100GGDNA,
 R5F100GHDNA, R5F100GJDNA, R5F100GKDNA, R5F100GLDNA
 R5F101GADNA, R5F101GCDNA, R5F101GDDNA, R5F101GEDNA, R5F101GFDNA, R5F101GGDNA,
 R5F101GHDNA, R5F101GJDNA, R5F101GKDNA, R5F101GLDNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	P48K8-50-5B4-4	0.13



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
A	0.75±0.05
b	0.25 ^{+0.05} _{-0.07}
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

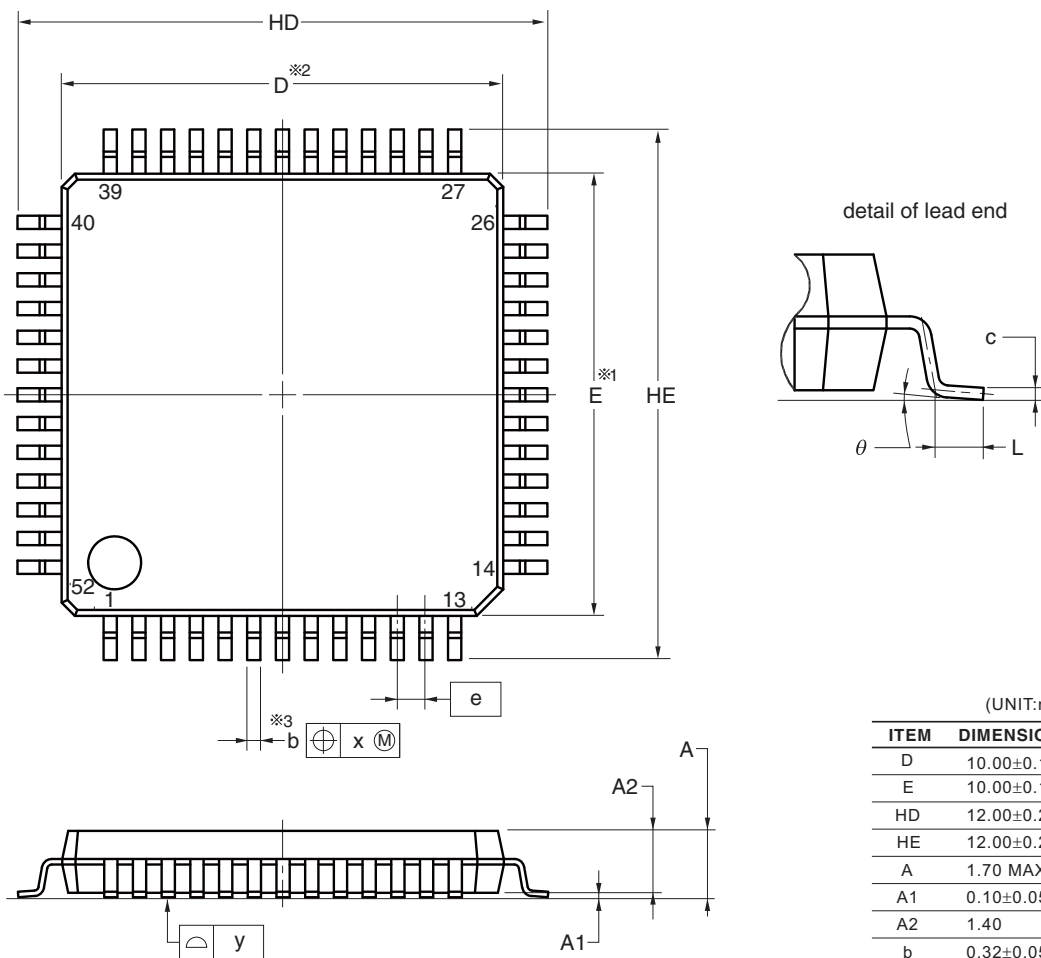
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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<R> 3.10 52-pin products

R5F100JCAFA, R5F100JDFA, R5F100JEFA, R5F100JFAFA, R5F100JGAFA, R5F100JHAFA, R5F100JJFA, R5F100JKFA, R5F100JLFA
 R5F101JCAFA, R5F101JDFA, R5F101JEFA, R5F101JFAFA, R5F101JGAFA, R5F101JHAFA, R5F101JJFA, R5F101JKFA, R5F101JLFA
 R5F100JCDA, R5F100JDDA, R5F100JEDA, R5F100JFDA, R5F100JGDA, R5F100JHDA, R5F100JDDA, R5F100JKDA, R5F100JLDA
 R5F101JCDA, R5F101JDDA, R5F101JEDA, R5F101JFDA, R5F101JGDA, R5F101JHDA, R5F101JDDA, R5F101JKDA, R5F101JLDA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
φ	0.65
x	0.13
y	0.10

NOTE

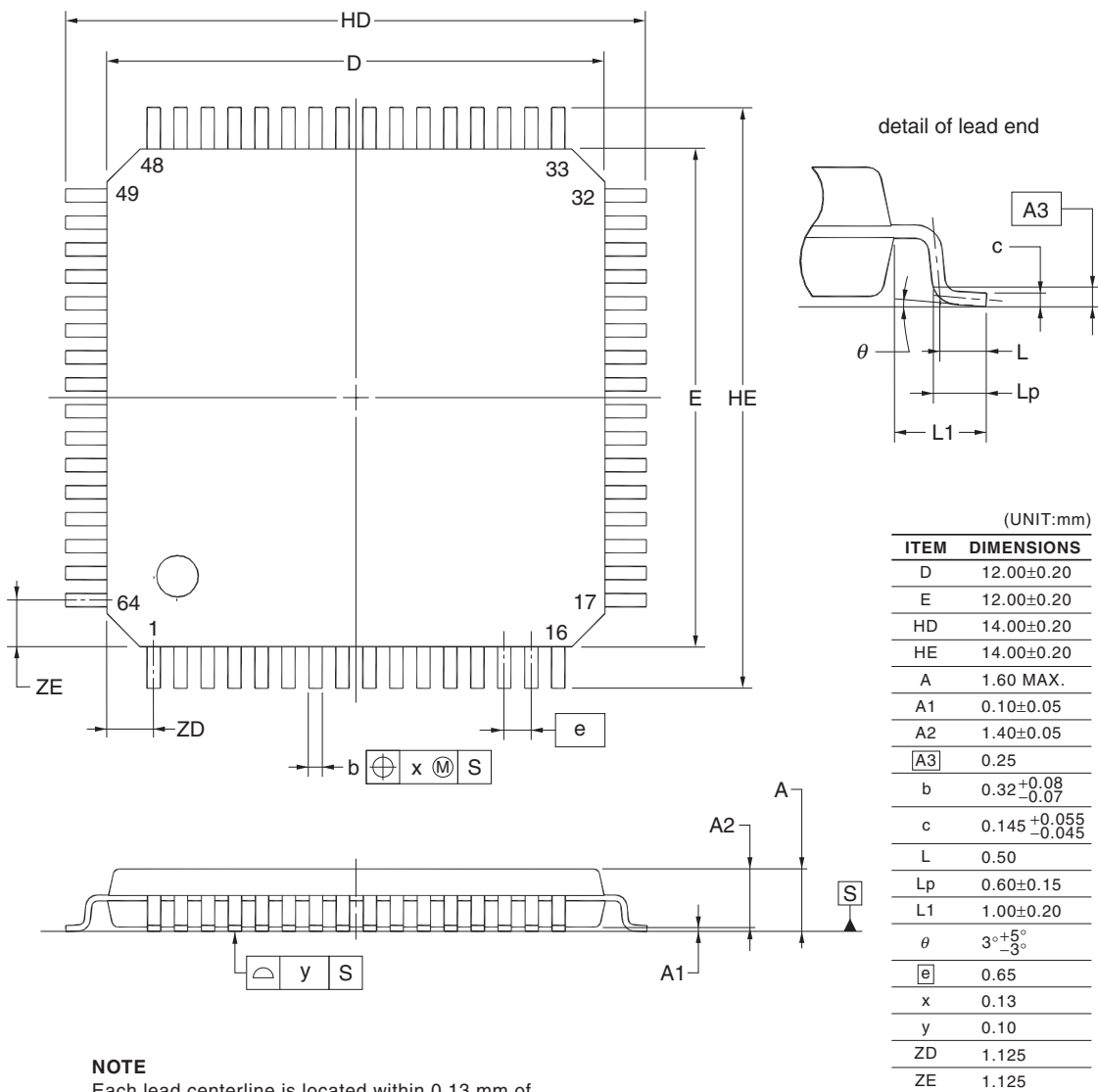
1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

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3.11 64-pin products

R5F100LCAFA, R5F100LDAFA, R5F100LEAFA, R5F100LFAFA, R5F100LGAFA, R5F100LHAFA, R5F100LJafa,
 R5F100LKafa, R5F100LLafa
 R5F101LCAFA, R5F101LDAFA, R5F101LEAFA, R5F101LFAFA, R5F101LGAFA, R5F101LHAFA, R5F101LJafa,
 R5F101LKafa, R5F101LLafa
 R5F100LCDFA, R5F100LDDFA, R5F100LEDFa, R5F100LFDFA, R5F100LGDFa, R5F100LHDFa, R5F100LJDFA,
 R5F100LKDFa, R5F100LLDFA
 R5F101LCDFA, R5F101LDDFA, R5F101LEDFa, R5F101LFDFA, R5F101LGDFa, R5F101LHDFa, R5F101LJDFA,
 R5F101LKDFa, R5F101LLDFA

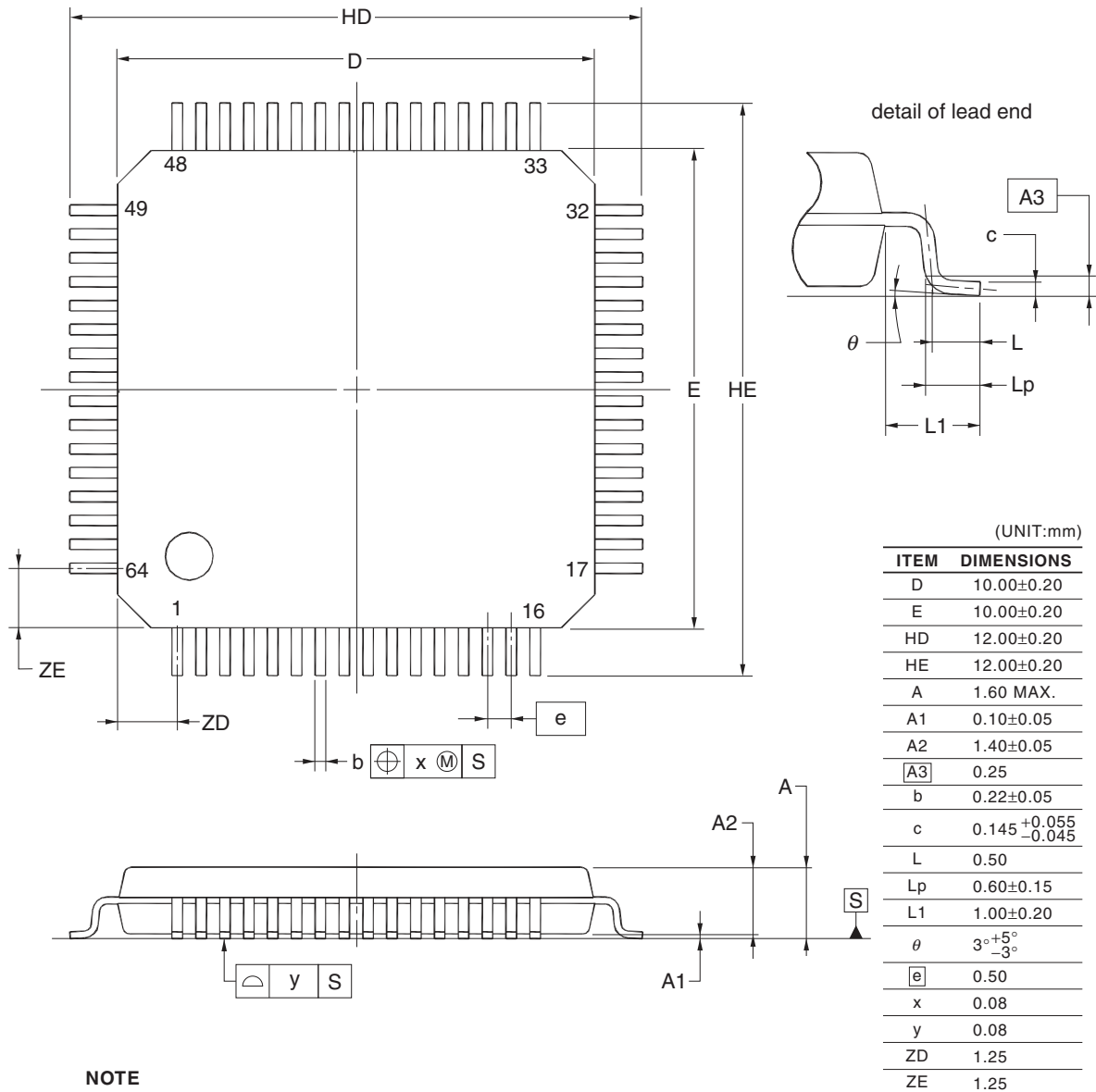
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



NOTE
 Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F100LCAFB, R5F100LDAFB, R5F100LEAFB, R5F100LFAFB, R5F100LGAFB, R5F100LHAFB, R5F100LJAFB, R5F100LKAFB, R5F100LLAFB
 R5F101LCAFB, R5F101LDAFB, R5F101LEAFB, R5F101LFAFB, R5F101LGAFB, R5F101LHAFB, R5F101LJAFB, R5F101LKAFB, R5F101LLAFB
 R5F100LCDFB, R5F100LDDFB, R5F100LEDFB, R5F100LDFDB, R5F100LGDFB, R5F100LHDFB, R5F100LJDFB, R5F100LKDFB, R5F100LLDFB
 R5F101LCDFB, R5F101LDDFB, R5F101LEDFB, R5F101LDFDB, R5F101LGDFB, R5F101LHDFB, R5F101LJDFB, R5F101LKDFB, R5F101LLDFB

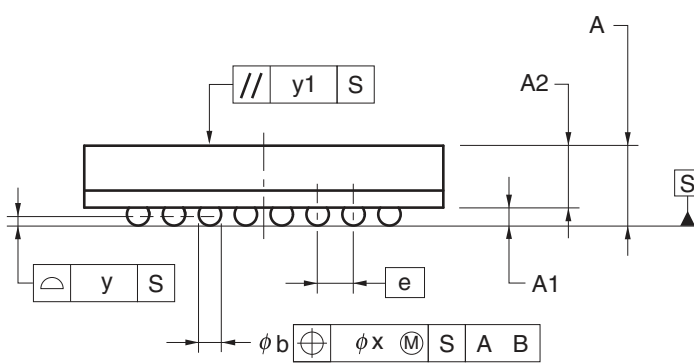
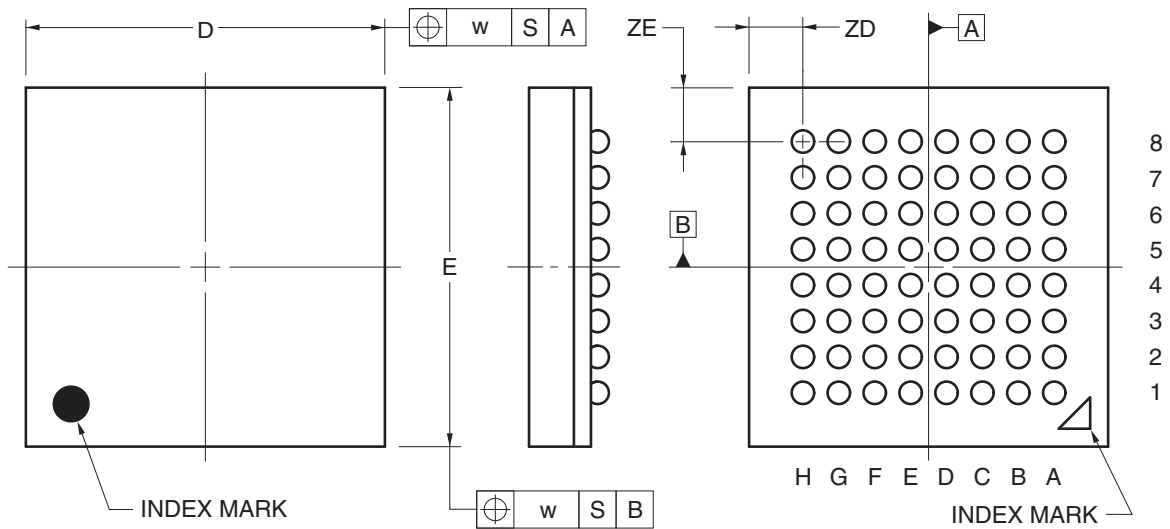
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F100LCABG, R5F100LDABG, R5F100LEABG, R5F100LFABG, R5F100LGABG, R5F100LHABG, R5F100LJABG
 R5F101LCABG, R5F101LDABG, R5F101LEABG, R5F101LFABG, R5F101LGABG, R5F101LHABG, R5F101LJABG
 R5F100LCDBG, R5F100LDDBG, R5F100LEDBG, R5F100LFDBG, R5F100LGDBG, R5F100LHDBG, R5F100LJDBG
 R5F101LCDBG, R5F101LDDBG, R5F101LEDBG, R5F101LFDBG, R5F101LGDBG, R5F101LHDBG, R5F101LJDBG

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-VFBGA64-4x4-0.40	PVBG0064LA-A	P64F1-40-AA2-2	0.03



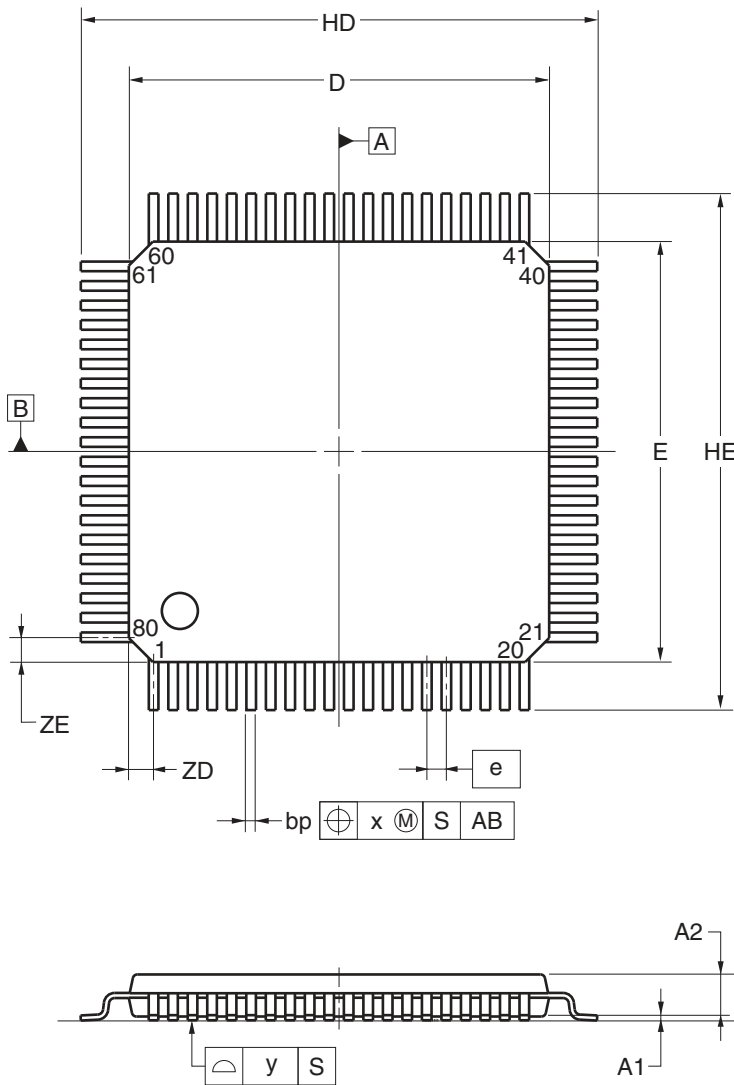
(UNIT:mm)

ITEM	DIMENSIONS
D	4.00±0.10
E	4.00±0.10
w	0.15
A	0.89±0.10
A1	0.20±0.05
A2	0.69
e	0.40
b	0.25±0.05
x	0.05
y	0.08
y1	0.20
ZD	0.60
ZE	0.60

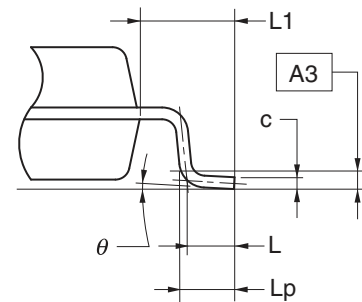
<R> 3.12 80-pin products

R5F100MFAFA, R5F100MGafa, R5F100MHAFA, R5F100MJafa, R5F100MKafa, R5F100MLafa
 R5F101MFAFA, R5F101MGafa, R5F101MHAFA, R5F101MJafa, R5F101MKafa, R5F101MLafa
 R5F100MFDFA, R5F100MGDFA, R5F100MHDFA, R5F100MJDFA, R5F100MKDFA, R5F100MLDFA
 R5F101MFDFA, R5F101MGDFA, R5F101MHDFA, R5F101MJDFA, R5F101MKDFA, R5F101MLDFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69



detail of lead end

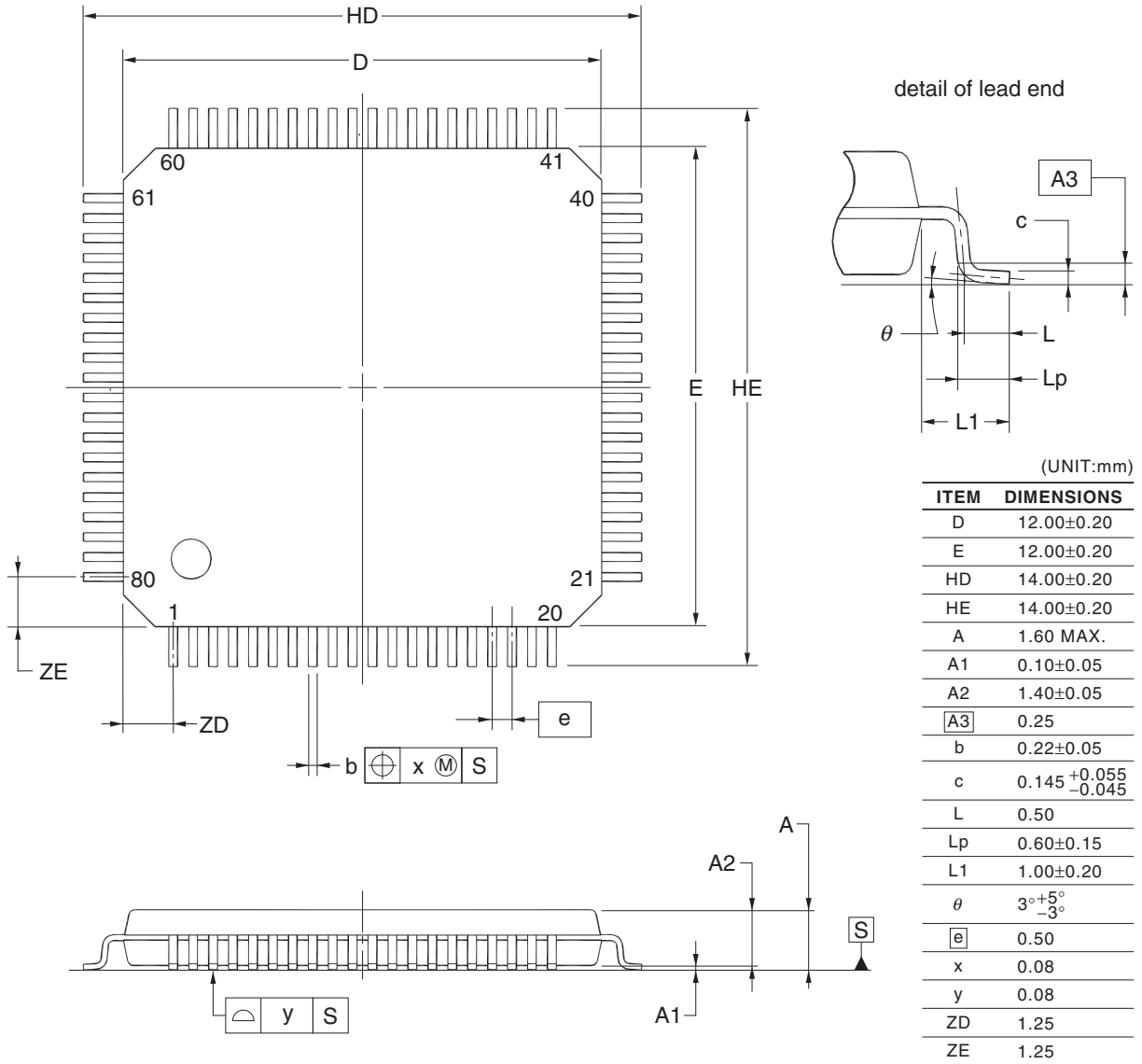


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.80	14.00	14.20
E	13.80	14.00	14.20
HD	17.00	17.20	17.40
HE	17.00	17.20	17.40
A	—	—	1.70
A1	0.05	0.125	0.20
A2	1.35	1.40	1.45
A3	—	0.25	—
bp	0.26	0.32	0.38
c	0.10	0.145	0.20
L	—	0.80	—
Lp	0.736	0.886	1.036
L1	1.40	1.60	1.80
theta	0°	3°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
ZD	—	0.825	—
ZE	—	0.825	—

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R5F100MFAFB, R5F100MGAFB, R5F100MHAFB, R5F100MJAFB, R5F100MKAFB, R5F100MLAFB
 R5F101MFAFB, R5F101MGAFB, R5F101MHAFB, R5F101MJAFB, R5F101MKAFB, R5F101MLAFB
 R5F100MDFB, R5F100MGDFB, R5F100MHDFB, R5F100MJDFB, R5F100MKDFB, R5F100MLDFB
 R5F101MDFB, R5F101MGDFB, R5F101MHDFB, R5F101MJDFB, R5F101MKDFB, R5F101MLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53

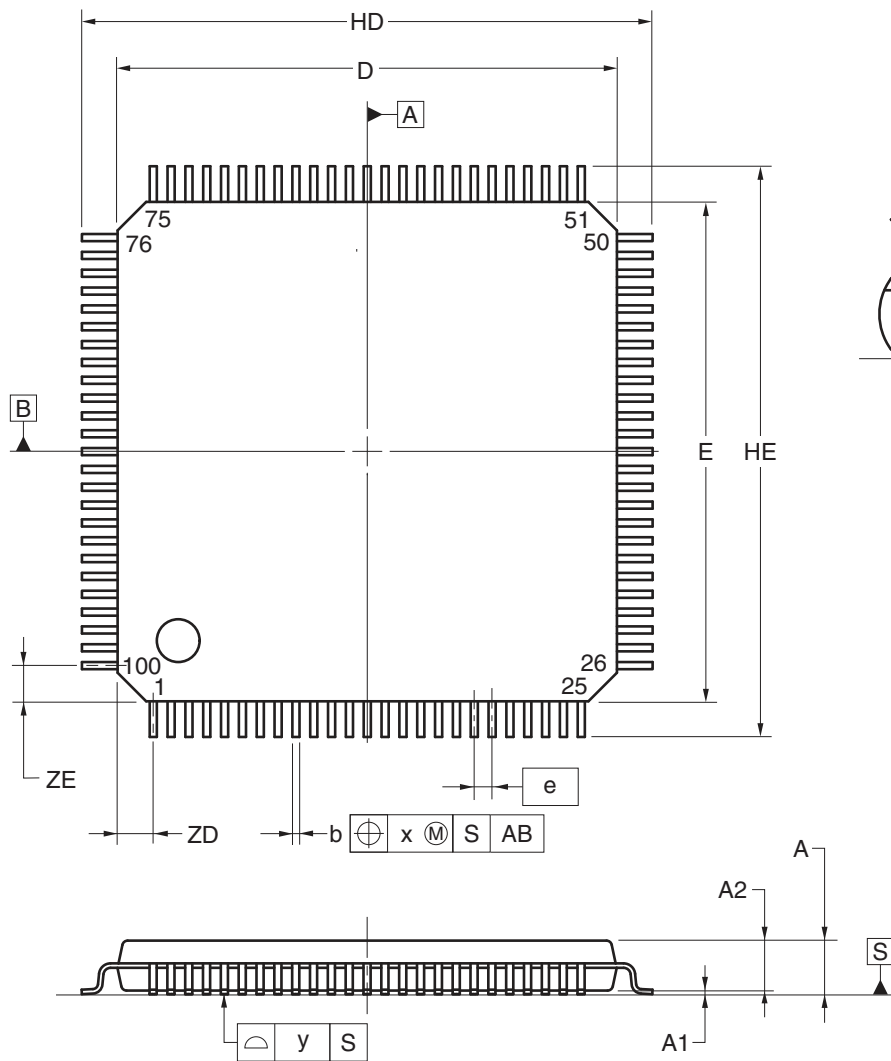


NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

3.13 100-pin products

R5F100PFAFB, R5F100PGAFA, R5F100PHAFA, R5F100PJAFB, R5F100PKAFB, R5F100PLAFB
 R5F101PFAFB, R5F101PGAFA, R5F101PHAFA, R5F101PJAFB, R5F101PKAFB, R5F101PLAFB
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFB, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFB, R5F101PKDFA, R5F101PLDFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



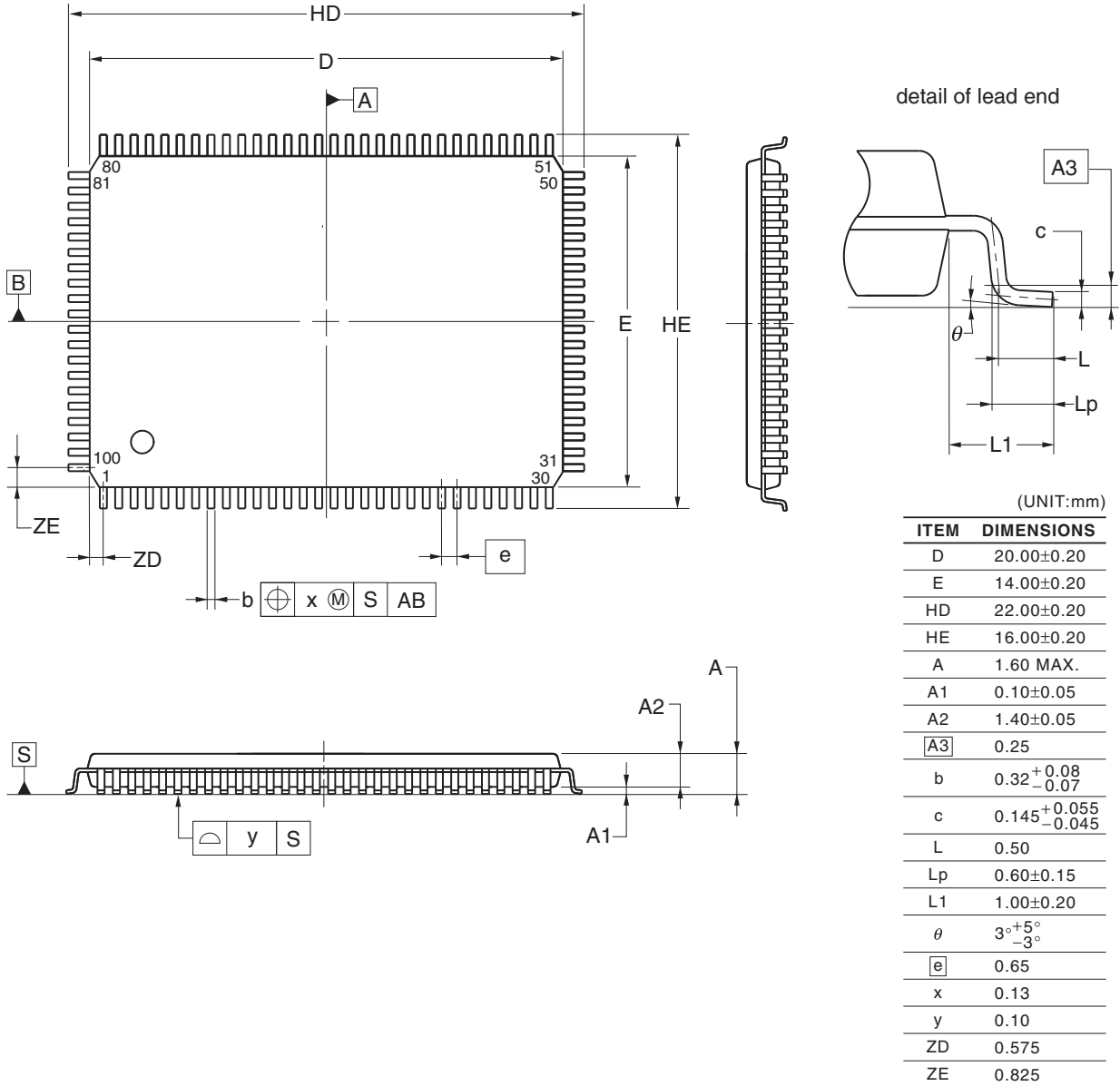
(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.20
E	14.00±0.20
HD	16.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	1.00
ZE	1.00

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R5F100PFAFA, R5F100PGAFA, R5F100PHAFA, R5F100PJAJA, R5F100PKAFA, R5F100PLAFA
 R5F101PFAFA, R5F101PGAFA, R5F101PHAFA, R5F101PJAJA, R5F101PKAFA, R5F101PLAFA
 R5F100PFDFA, R5F100PGDFA, R5F100PHDFA, R5F100PJDFA, R5F100PKDFA, R5F100PLDFA
 R5F101PFDFA, R5F101PGDFA, R5F101PHDFA, R5F101PJDFA, R5F101PKDFA, R5F101PLDFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92

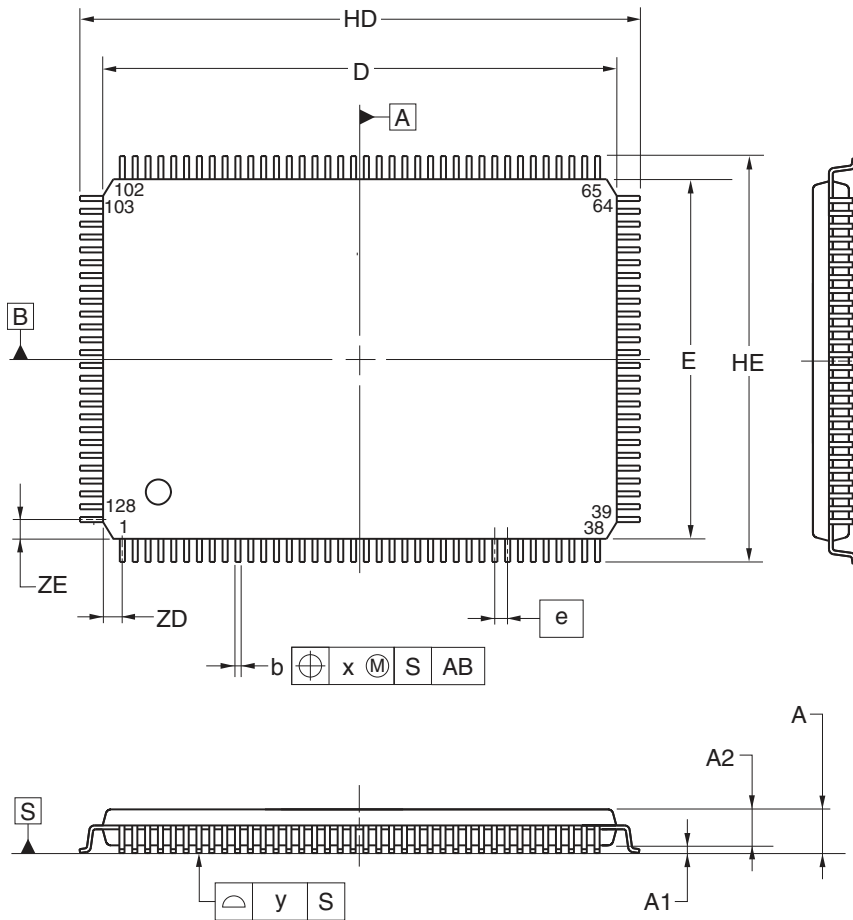


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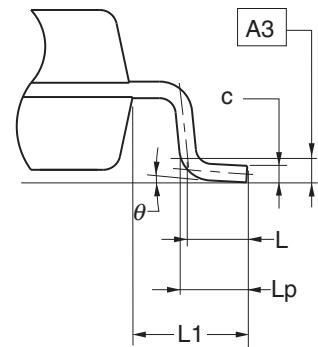
3.14 128-pin products

R5F100SHAFB, R5F100SJAFB, R5F100SKAFB, R5F100SLAFB
 R5F101SHAFB, R5F101SJAFB, R5F101SKAFB, R5F101SLAFB
 R5F100SHDFB, R5F100SJDFB, R5F100SKDFB, R5F100SLDFB
 R5F101SHDFB, R5F101SJDFB, R5F101SKDFB, R5F101SLDFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

Revision History	RL78/G13 Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 29, 2012	-	First Edition issued
2.00	Oct 12, 2012	7	Figure 1-1. Part Number, Memory Size, and Package of RL78/G13: Pin count corrected.
		25	1.4 Pin Identification: Description of pins INTP0 to INTP11 corrected.
		40, 42, 44	1.6 Outline of Functions: Descriptions of Subsystem clock, Low-speed on-chip oscillator, and General-purpose register corrected.
		41, 43, 45	1.6 Outline of Functions: Lists of Descriptions changed.
		59, 63, 67	Descriptions of Note 8 in a table corrected.
		68	(4) Common to RL78/G13 all products: Descriptions of Notes corrected.
		69	2.4 AC Characteristics: Symbol of external system clock frequency corrected.
		96 to 98	2.6.1 A/D converter characteristics: Notes of overall error corrected.
		100	2.6.2 Temperature sensor characteristics: Parameter name corrected.
		104	2.8 Flash Memory Programming Characteristics: Incorrect descriptions corrected.
		116	3.10 52-pin products: Package drawings of 52-pin products corrected.
		120	3.12 80-pin products: Package drawings of 80-pin products corrected.

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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