TPS56637 4.5-V to 28-V Input, 6-A Synchronous Buck Converter

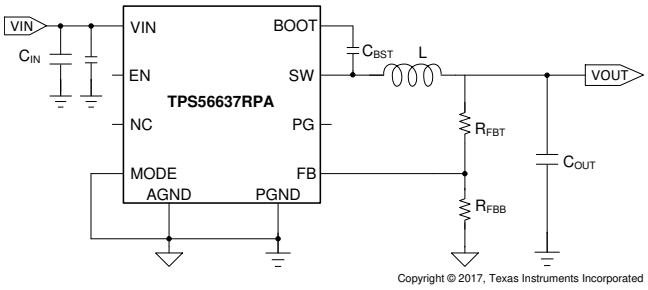
1 Features

- 4.5-V to 28-V input voltage range
- 0.6-V to 13-V output voltage range
- 6-A maximum continuous output current
- Integrated 26-mΩ and 12-mΩ MOSFETs
- 0.6-V ±1% Reference Voltage
- D-CAP3™ control mode for fast transient response
- Eco-mode™ and FCCM (forced continuous conduction mode) selectable for light-load operation through MODE pin
- Internal 2-ms soft start
- Built-in output discharge function
- 500-kHz switching frequency
- Power good indicator to monitor output voltage
- Cycle by cycle over current limit
- Non-latched protections for UV, OV, OT and UVLO
- –40°C to +150°C operating junction temperature
- Small 10-Pin 3.0-mm × 3.0-mm HotRod™ QFN Package
- Available in WEBENCH® Power Designer to create custom designs

2 Applications

- Enterprise systems: multifunction printers, storage
- Personal electronics: TVs, speakers, set-top box, portable electronics
- Industrial applications: electronic point of sale, factory automation and control, motor drives
- General purposes for 12-V,19-V, 24-V power-bus supply

Simplified Schematic



3 Description

The TPS56637 is a high efficiency, high-voltage input, easy-to-use synchronous buck converter with integrated MOSFETs.

With the wide operating input voltage range of 4.5 V to 28 V, the TPS56637 is ideally suited for systems powered from 12-V, 19-V, 24-V power-bus rails. It supports up to 6-A continuous output current at output voltages between 0.6 V and 13 V.

The TPS56637 uses DCAP3™ control mode to provide fast transient response, good line and load regulation, no requirement for external compensation, and supports low equivalent series resistance (ESR) output capacitors such as POSCAP and MLCC.

The TPS56637 has both FCCM and Eco-mode™ operation modes for selection at light-load condition through configuration of MODE pin. To attain high efficiency at light load, Eco-mode™ could be selected. To support tight output voltage ripple requirement, FCCM could be selected.

The TPS56637 provides complete non-latched OV (Over-voltage), UV (Under-voltage), OC (Over-current), OT (Over-temperature) and UVLO (Under-voltage lock-out) protections combined with power good indicator and output discharge function features.

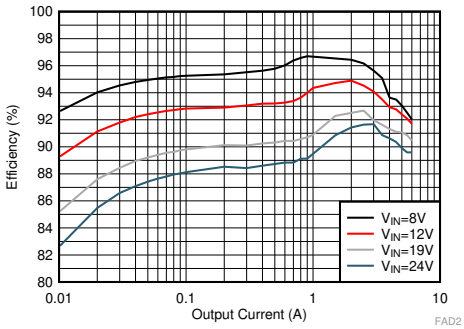
The TPS56637 is available in a 10-pin 3.0-mm x 3.0-mm HotRod™ QFN package and the junction temperature is specified from –40°C to 150°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS56637	VQFN-HR (10)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency vs Output Current V_{OUT} = 5 V



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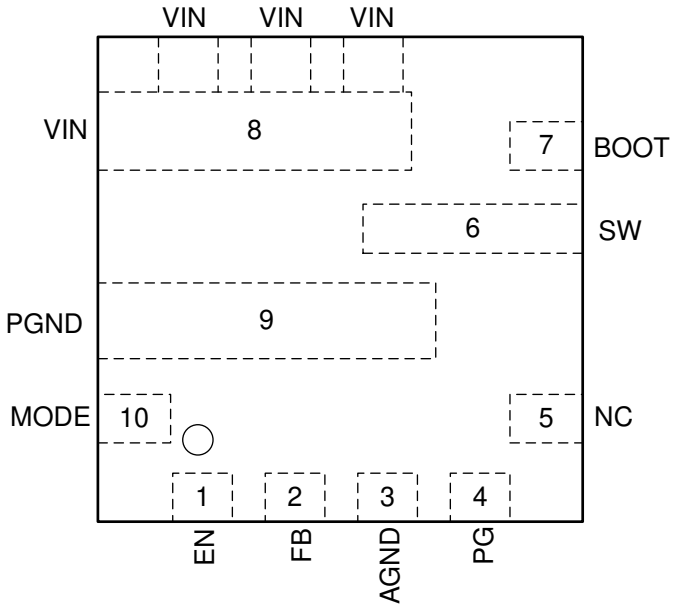
4 Revision History

Changes from Original (July 2018) to Revision A **Page**

- Changed marketing status from Advance Information to production data. ... 1

5 Pin Configuration and Functions

RPA Package
10-Pin VQFN-HR
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND	3	G	Ground of internal analog circuitry. Connect AGND to PGND plane at a single point.
BOOT	7	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1-µF bootstrap capacitor between BOOT and SW.
EN	1	I	Enable input control. Driving EN high or leaving this pin floating enables the converter. A resistor divider can be used to imply an UVLO function.
FB	2	I	Output feedback. Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage.
MODE	10	I	Operation mode selection pin. Leaving this pin floating(≥500 kΩ) forces the TPS56637 into FCCM. Connecting this pin to GND(≤10 kΩ) forces the TPS56637 into Eco-mode™ under light load.
NC	5	N	Not Connected, keep this pin floating.
PG	4	O	Open Drain Power Good Indicator, it is asserted low if output voltage is out of PG threshold due to over-voltage, under-voltage, thermal shutdown, EN shutdown or during soft-start.
PGND	9	G	Power GND terminal. Source terminal of low side MOSFET.
SW	6	O	Switching node terminal. Connect the output inductor to this pin with wide and short tracks
VIN	8	P	Input voltage supply pin. Drain terminal of high-side MOSFET. Connect the input decoupling capacitors between VIN and GND.

6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	V_{IN}	–0.3	32	V
	BOOT	–0.3	SW+6	V
	BOOT-SW	–0.3	6.0	V
	EN, FB, MODE	–0.3	6.0	V
	PGND, AGND	–0.3	0.3	V
Output voltage	SW	–0.3	32	V
	SW (<10 ns transient)	–4	32.5	V
	PG	-0.3	6	V
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 Handling Ratings

			VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 150°C (unless otherwise noted).(1)

		MIN	NOM	MAX	UNIT
Input Voltage	V_{IN}	4.5		28	V
	BOOT	4.5		33.5	V
	BOOT-SW	-0.1		5.5	V
	EN, FB, MODE	-0.1		5.5	V
	PGND, AGND	-0.1		0.1	V
Output Voltage	SW	-0.1		28	V
	PG	-0.1		5.5	V
Operating junction temperature, T_J		-40		150	°C

(1) Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications, see Electrical Characteristics

6.4 Thermal Information

THERMAL METRIC(1)		TPS56637 QFN HOTROD 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	16.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	16.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 12 V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5 V to 28 V(unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_Q	Quiescent current, Operating at ULQ mode(1)			140		µA
I_{SD}	Shutdown supply current	T_J=25°C, V_{EN}=0 V		2		µA
UVLO						
UVLO	V_{IN} Under-Voltage Lockout	Wake up V_{IN} voltage	4.0	4.2	4.4	V
		Shut down V_{IN} voltage	3.6	3.7	3.8	V
		Hysteresis V_{IN} voltage		500		mV
ENABLE(EN PIN)						
I_{EN_INPUT}	Input current	V_{EN} = 1.1V		1		µA
I_{EN_HYS}	Hysteresis current	V_{EN} = 1.3V		4		µA
$V_{EN(ON)}$	Enable threshold	EN rising		1.18	1.26	V
$V_{EN(OFF)}$		EN failling	1.04	1.12		V
FEEDBACK VOLTAGE						
V_{FB}	Feedback voltage	V_{OUT} = 5V, continuous mode operation, T_J=25°C	0.594	0.6	0.606	V
		V_{OUT} = 5V, continuous mode operation, T_J=-40°C to 150°C	0.591	0.6	0.609	V
MOSFET						
$R_{DS(on)h}$	High side switch resistance	T_J = 25°C, V_{BST} - V_{SW} = 5 V		26		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_J = 25°C		12		mΩ
CURRENT LIMIT						
I_{OCL}	Valley current limit		6.3	7.5	8.6	A
I_{OC_REV}	Reverse current limit for FCCM Mode		2.3	3	3.7	A
POWER GOOD						
V_{PGTH}	PG lower threshold - falling	% of V_{FB}		85%		
	PG lower threshold - rising	% of V_{FB}		90%		
	PG upper threshold - falling	% of V_{FB}		110%		
	PG upper threshold - rising	% of V_{FB}		115%		
I_{PGSINK}	PG sink current	V_{FB} = 0.5V, V_{PG} = 0.5V		1.5		mA
I_{PGLK}	PG leakage current	V_{PG} = 5.5V	-1		1	µA
FREQUENCY						
F_{SW}	Switching frequency	V_{OUT} =5V, continuous mode operation		500		kHz
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP threshold	OVP detect(L>H)		125%		
		Hysteresis		5%		
V_{UVP}	Output UVP threshold	Hiccup detect(H>L)		65%		
		Hysteresis		5%		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold(2)	Temperature Rising		165		°C
		Hysteresis		30		°C
SW DISCHARGE RESISTANCE						
R_{DISCHG}	V_{OUT} discharge resistance	V_{EN}=0, V_{SW}=0.5V, T_J=25°C		200		Ω

(1) Not representative of the total input current of the system when in regulation. Ensured by design and characterization test.
(2) Not production tested. Ensured by design and engineering sample correlation.

6.6 Timing Requirements

The electrical ratings specified in this section apply to all specifications in this document unless otherwise noted. These specifications are interpreted as conditions that will not degrade the parametric or functional specifications of the device for the life of the product containing it. Typical values correspond to T_J = 25°C, V_{IN} = 12 V. Minimum and maximum limits are based on T_J = –40°C to +150°C, V_{IN} = 4.5 V to 28 V(unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
$t_{ON(MIN)}$	Minimum on time(1)			50		ns
$t_{OFF(MIN)}$	Minimum off time	V_{FB} = 0.5 V, measure SW at 50% V_{IN}, Eco-mode		200	300	ns
SOFT START						
T_{SS}	Soft start time	Internal soft-start time		2		ms
OUTPUT UNDERVOLTAGE PROTECTION						
T_{UVP_WAIT}	UV protection hiccup wait time	UV triggered (V_{FB} lower than 65% V_{FB_nom})		0.25		ms
T_{UVP_HICCUP}	UV protection hiccup time before recovery			25		ms

(1) Not production tested. Ensured by design and engineering sample correlation.

6.7 Typical Characteristics

V_{IN} = 12 V (unless otherwise noted)

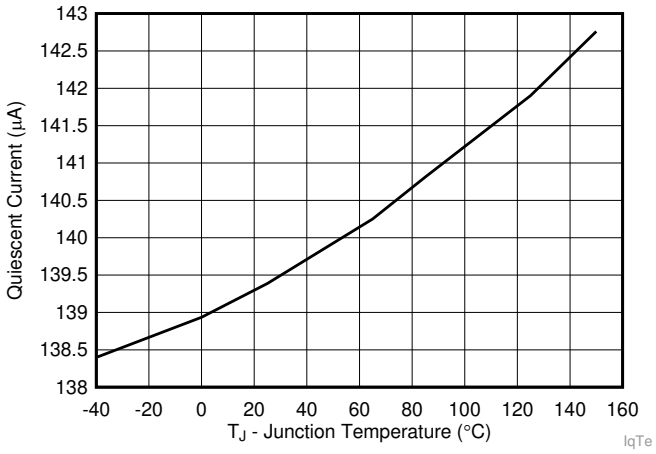


Figure 1. Quiescent Current vs Temperature

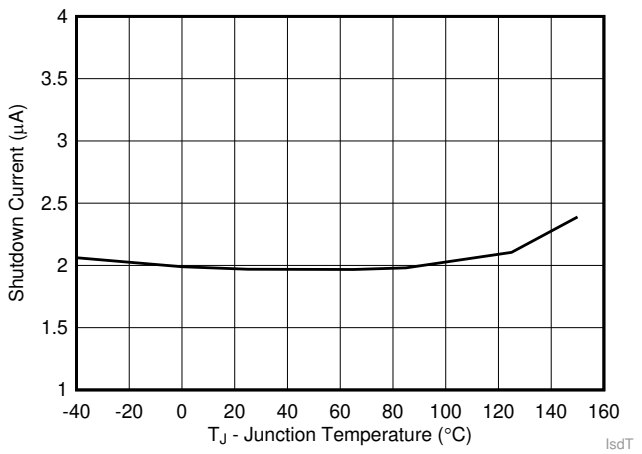


Figure 2. Shutdown Current vs Temperature

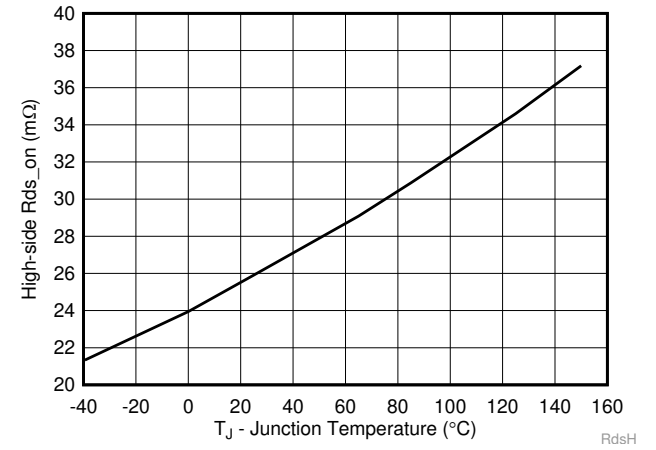


Figure 3. High-Side $R_{DS(on)}$ vs Temperature

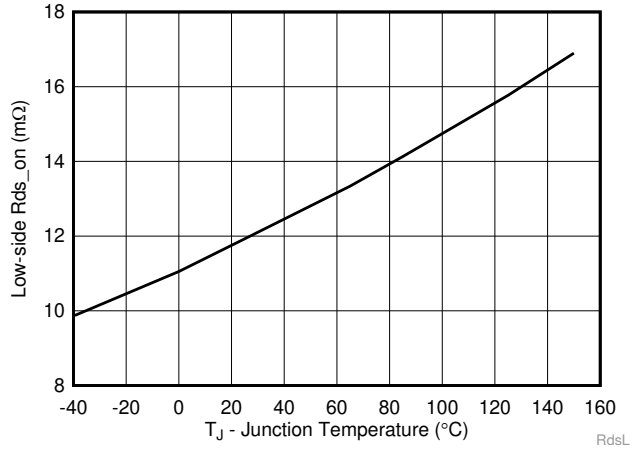


Figure 4. Low-side $R_{DS(on)}$ vs Temperature

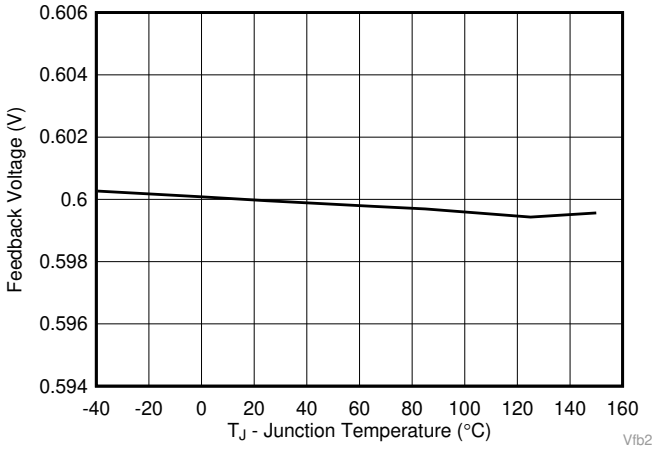


Figure 5. Feedback Voltage vs Temperature

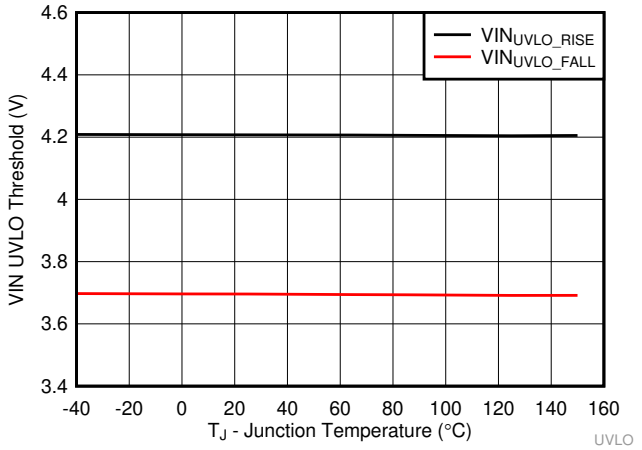


Figure 6. VIN UVLO Threshold vs Temperature

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

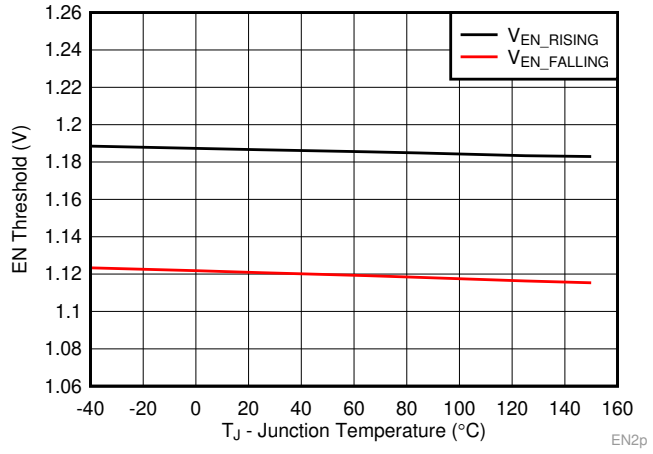


Figure 7. EN Threshold vs Temperature

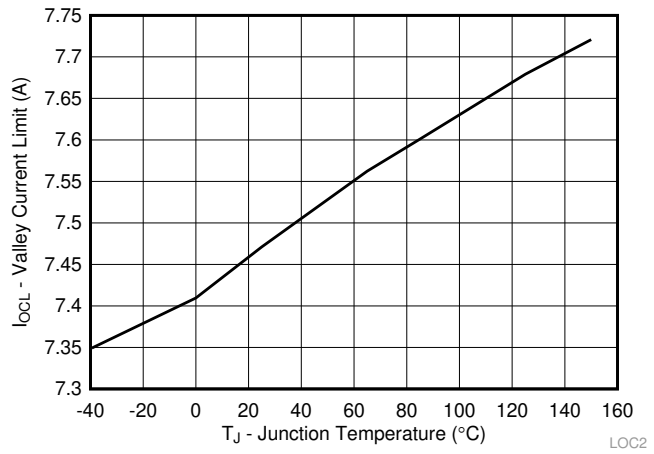


Figure 8. Valley Current Limit vs Temperature

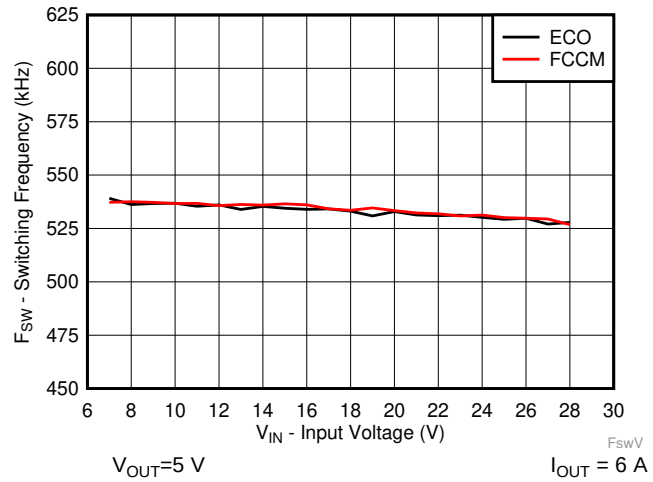


Figure 9. Switching Frequency vs Input voltage

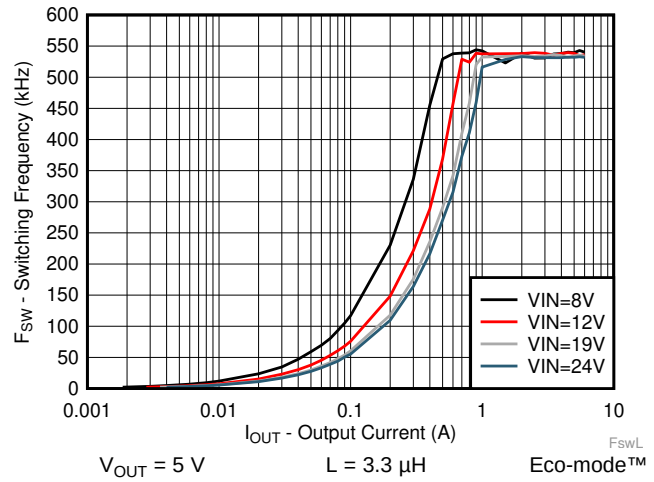


Figure 10. Switching Frequency vs Output Current

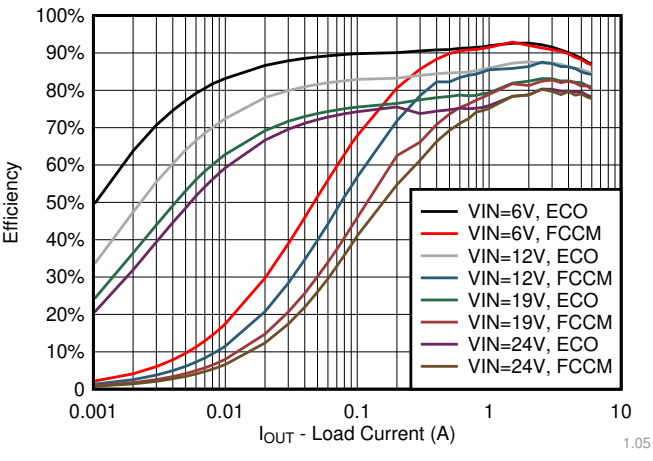


Figure 11. VOUT = 1.05 V Efficiency, L = 1 µH

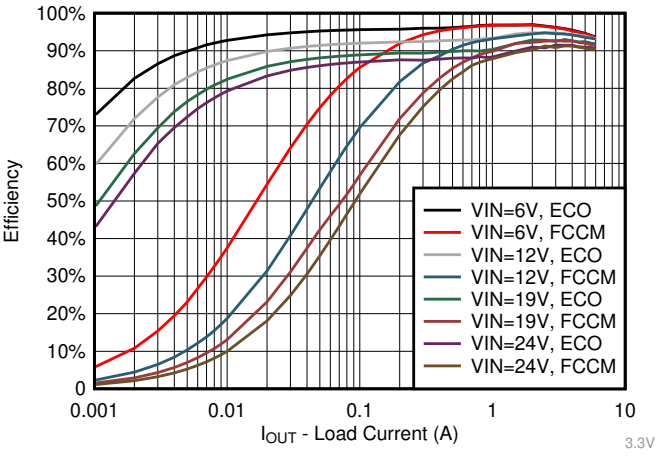


Figure 12. VOUT = 3.3 V Efficiency, L = 2.2 µH

Typical Characteristics (continued)

V_{IN} = 12 V (unless otherwise noted)

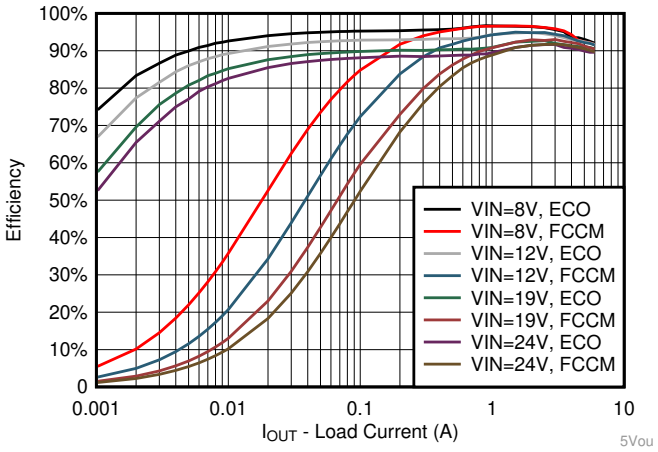


Figure 13. VOUT = 5 V Efficiency, L = 3.3 µH

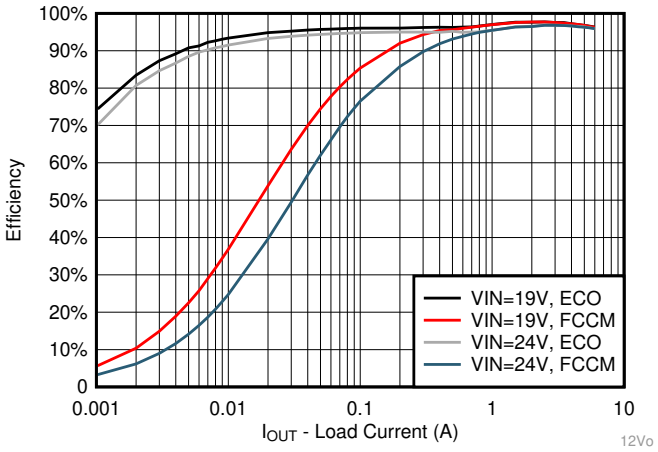


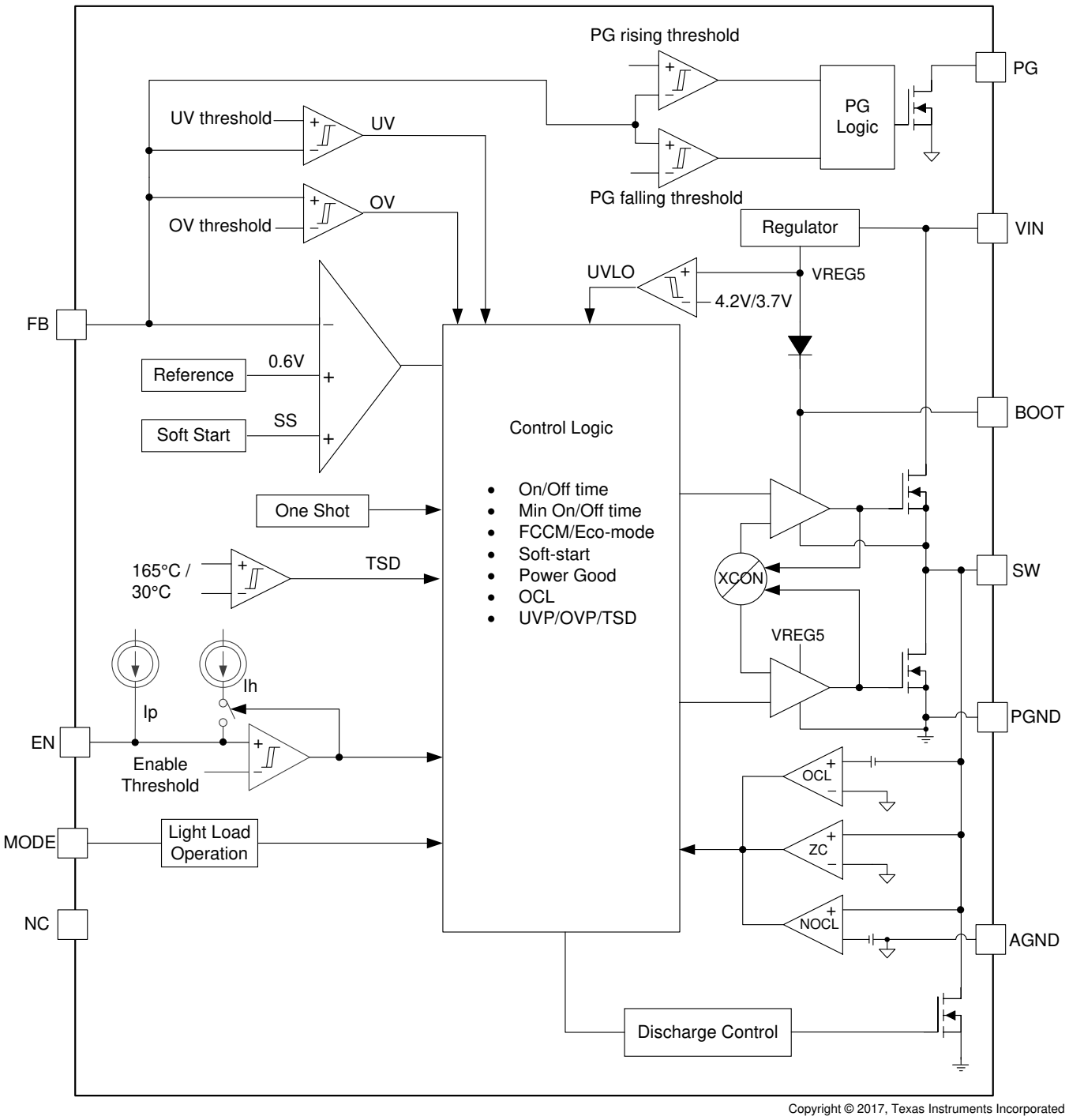
Figure 14. VOUT = 12 V Efficiency, L = 5.6 µH

7 Detailed Description

7.1 Overview

The TPS56637 is a 6-A synchronous buck converter operating from 4.5V to 28V input voltage (V_{IN}), and its output voltage ranges from 0.6V to 13V. The proprietary D-CAP3™ mode enables low external component count, ease of design, optimization of the power design for power, size and efficiency. The device employs D-CAP3™ mode control that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between CCM operating mode at higher load condition and DCM operation at lighter load condition. Eco-mode™ allows the TPS56637 to maintain high efficiency at light load. FCCM mode has the quasi-fixed switching frequency at both light and heavy load. The TPS56637 is able to adapt both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 The Adaptive On-Time Control and PWM Operation

The main control loop of the TPS56637 is adaptive on-time pulse width modulation (PWM) controller that supports a proprietary DCAP3™ mode control. The DCAP3™ mode control combines adaptive on-time control with an internal compensation circuit for quasi-fixed frequency and low external component count configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output. The TPS56637 also includes an error amplifier that makes the output voltage very accurate. No external current sense network or loop compensation is required for DCAP3™ control topology.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one-shot timer expires. This one-shot duration is set proportional to the output voltage, V_{OUT}, and is inversely proportional to the converter input voltage, V_{IN}, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. When the feedback voltage falls below the reference voltage, the one-shot timer is reset and the high-side MOSFET is turned on again . An internal ripple generation circuit is added to reference voltage for emulating the output ripple, and this enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC).

7.3.2 Mode Selection

TPS56637 has a MODE pin that can offer 2 different states of operations under light load condition. If MODE pin is short to GND(≤10kΩ), TPS56637 works under Eco-mode™ control scheme. If MODE pin is floating(≥500kΩ), TPS56637 works under FCCM mode.

Figure 15 below shows the typical start-up sequence of the device once the enable signal triggers the EN turn-on threshold. After the voltage of internal VCC crosses the UVLO rising threshold, it takes about 64µs to finish the reading and setting of MODE. After this process, the MODE is latched and will not change until V_{IN} or EN toggles to restart-up this device. Then after a delay of around 650µs the internal soft-start function begins to ramp up the reference voltage to the PWM comparator.

Table 1. MODE Pin Settings

MODE Pin	Light Load Operation Mode
Short to GND (≤10kΩ)	Eco-mode™
Floating (≥500kΩ)	FCCM

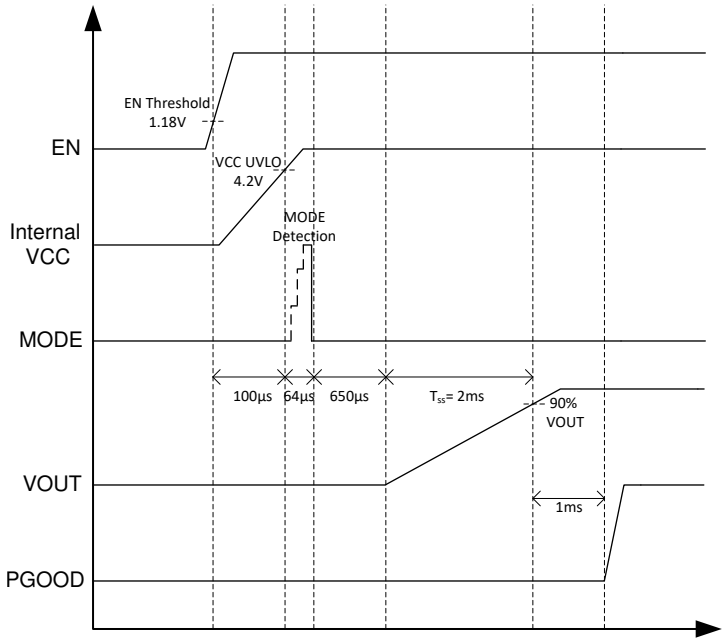


Figure 15. Power-Up Sequence

7.3.2.1 Eco-mode™ Control Scheme

When MODE pin is short to GND(≤10kΩ), the TPS56637 is set to Eco-mode™ control scheme to maintain high light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to a point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when the zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that longer time is needed to discharge the output capacitor with smaller load current to the level of the reference voltage. This process makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation $I_{OUT(LL)}$ current can be calculated by Equation 1.

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot f_{SW}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

7.3.2.2 FCCM Control

When MODE pin is floating(≥500kΩ), the TPS56637 is set to operate in forced continuous conduction mode (FCCM) in light load conditions and allows the inductor current to become negative. In FCCM, the switching frequency is maintained at a quasi-fixed level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load compared with which under Eco-mode™. This mode also can help to avoid switching frequency dropping into audible range that may introduces some audible "noise".

7.3.3 Soft Start and Pre-Biased Soft Start

The TPS56637 features an internal 2-ms soft-start function. The internal soft start circuitry controls the output voltage slope during startup. This avoids excessive inrush current and ensures a controlled output voltage rise time. It also prevents unwanted voltage drops from high impedance power sources or batteries. When EN pin is set to start device operation, the internal soft-start circuitry will begin ramping up the reference voltage to the PWM comparator with a controlled slope. If the output capacitor is pre-biased at startup, the device initiates switching and start ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.4 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin voltage exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the standby operation.

The EN pin has an internal pull-up current source which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, open-drain or open-collector output logic can be used to interface with the pin.

The TPS56637 implements internal undervoltage-lockout (UVLO) circuitry on the V_{IN} pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 500 mV.

If an application requires a higher UVLO threshold on the VIN pin, then the EN pin can be configured as shown in Figure 16. When using the external UVLO function, setting the hysteresis at a value greater than 500 mV is recommended.

The EN pin has a small pull-up current, I_p, which sets the default state of the pin to enable when no external components are connected. The pull-up current is also used to control the voltage hysteresis for the UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use Equation 2 , and Equation 3 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1, R2 were settled down, the V_{EN} voltage can be calculated by Equation 4, which should be lower than 5.5V with max V_{IN}.

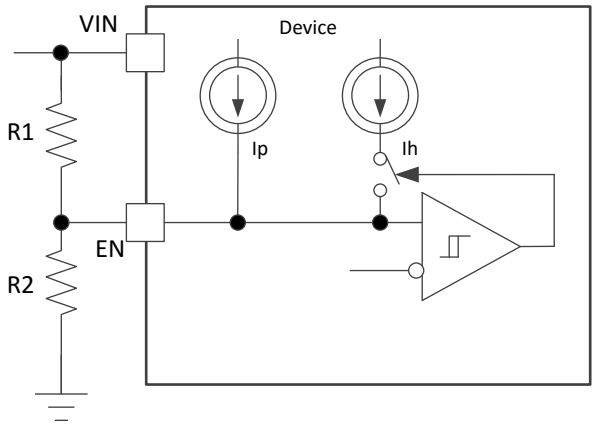


Figure 16. Adjustable VIN Undervoltage Lockout

$$R_1 = \frac{V_{START}\frac{V_{ENfalling}}{V_{ENrisig}} - V_{STOP}}{I_p\left(1 - \frac{V_{ENfalling}}{V_{ENrising}}\right) + I_h} \quad (2)$$

$$R_2 = \frac{R_1 \times V_{ENfalling}}{V_{STOP} - V_{ENfalling} + R_1\left(I_p + I_h\right)} \quad (3)$$

$$V_{EN} = \frac{R_2 \times V_{IN} + R_1 R_2\left(I_p + I_h\right)}{R_1 + R_2} \quad (4)$$

Where

- I_p = 1 µA
- I_h = 4 µA
- $V_{ENfalling}$ = 1.12 V
- $V_{ENrising}$ = 1.18 V

7.3.5 Output Overcurrent Limit and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle by cycle valley detect control circuit. The switching current is monitored during off state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switching current. To improve accuracy, the voltage sensing is temperature compensated.

During the on-time of the high-side FET switch, the switching current increases at a linear rate determined by V_{IN}, V_{OUT}, the on-time and the output inductor value. During the on-time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the monitored current is above the OCL level, the converter maintains low-side FET on and delays the creation of a new set pulse, even the voltage feedback loop requires one, until the current level becomes OCL level or lower. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner.

There are some important considerations for this type of over current limit. When the load current is higher than the over current threshold by one half of the peak-to-peak inductor ripple current, the OCL is triggered and the current is being limited, output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 65% of the target voltage, the UVP comparator detects it and shuts down the device after a deglitch wait time of 0.25ms and then re-start after the hiccup time of 25ms. When the over current condition is removed, the output will be recovered.

7.3.6 Overvoltage Protection

When the output voltage becomes higher than 125% of the target voltage, the OVP comparator output goes high after a deglitch time of 256µs and then the output will be discharged. When the over voltage condition is removed, the discharge path will still be on for a hiccup time of 25ms before a re-soft-start process to recover the output voltage.

7.3.7 UVLO Protection

Undervoltage Lockout protection(UVLO) monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut down. This protection is non-latched.

7.3.8 Thermal Shutdown

The junction temperature (T_j) of the device is monitored by an internal temperature sensor. If T_j exceeds 165°C (typical), the device goes into thermal shut down. Both the high-side and low-side power FETs are turned off and the discharge path is turned on. When T_j decreases below the hysteresis amount, the converter resumes normal operation, beginning with Soft Start. To avoid unstable conditions, a hysteresis of typically 30°C is implemented on the thermal shut down temperature.

7.3.9 Output Voltage Discharge

The TPS56637 has a built in discharge function by using an integrated MOSFET with 200-Ω $R_{DS(on)}$, which is connected to the output terminal SW. The discharge is slow due to the lower current capability of the MOSFET. The discharge path will be turned on when the device is turned off due to UV, OV, OT and EN shut down conditions.

7.3.10 Power Good

The TPS56637 has a built in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for startup sequencing of multiple rails. The PG pin is an open-drain output that requires a pull-up resistor (to any voltage below 5.5 V). A pull-up resistor of 100kΩ is recommended to pull it up to 5V voltage. It can sink 1.5mA of current and maintain its specified logic low level. Once the FB pin voltage is between 90% and 110% of the internal reference voltage (V_{REF}) and after a deglitch time of 64µs, the PG turns to high impedance status. The PG pin is pulled low after a deglitch time of 32µs when FB pin voltage is lower than 85% of the internal reference voltage or greater than 115% of the internal reference voltage, or in events of thermal shutdown, EN shutdown, UVLO conditions. V_{IN} must remain present for the PG pin to stay Low.

Table 2. Power Good Pin Logic Table (TPS56637)

Device State		PG Logic Status	
		High Impedance	Low
Enable (EN=High)	V_{FB} doesn't trigger V_{PGTH}	√	
	V_{FB} triggers V_{PGTH}		√
Shutdown (EN=Low)			√
UVLO	$2\ V < V_{IN} < V_{UVLO}$		√
Thermal Shutdown	$T_J > T_{SD}$		√
Power Supply Removal	$V_{IN} < 2\ V$	√	

7.4 Device Functional Modes

7.4.1 Standby Operation

The TPS56637 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 2μA(typical) when in standby condition.

7.4.2 Normal Operation

When the input voltage is above the UVLO threshold voltage and EN pin is high, TPS56637 can operate in its normal switching modes. Normal continuous conduction mode (CCM) occurs when the minimum switch current is above 0 A. In CCM, the TPS56637 operates at a quasi-fixed frequency of 500kHz (typical).

7.4.3 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency is maintained at an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in Eco-mode™ control scheme, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode™ control scheme maintains higher efficiency at light load with a lower switching frequency. If the TPS56637 works at Eco-mode™ and the load current is light enough to a specific value, the TPS56637 will enter ULQ mode that the TPS56637 will disable some internal circuits to further increase the light load efficiency.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The schematic of Figure 17 shows a typical application for TPS56637. This design converts an input voltage range of 8V to 28V down to 5V with a maximum output current of 6 A.

8.2 Typical Application

The application schematic in Figure 17 shows the TPS56637 8-V to 28-V Input, 5-V output converter design meeting the requirements for 6-A output. This circuit is available as the evaluation module (EVM). The sections provide the design procedure.

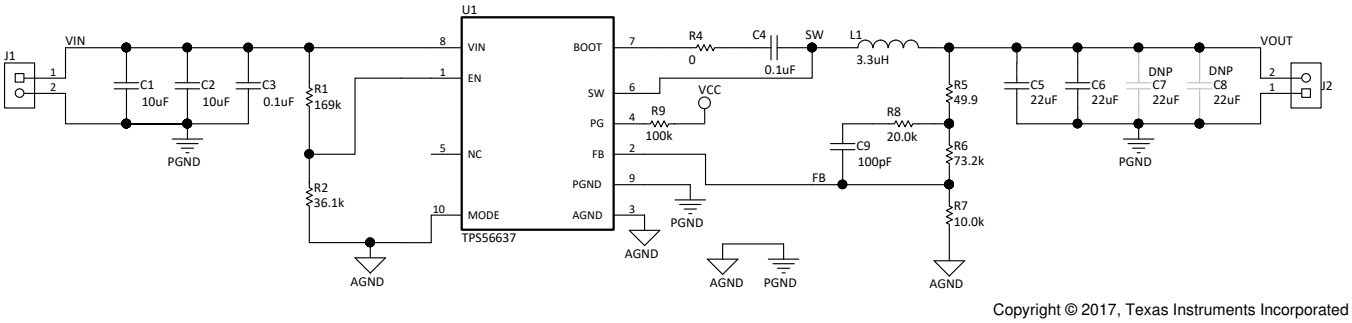


Figure 17. TPS56637 5-V, 6-A Reference Design

8.2.1 Design Requirements

Table 3 shows the design parameters for this application.

Table 3. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	24V nominal, 8V to 28V
Output voltage	5V
Transient response, 6-A load step	ΔV_{OUT} = ±5%
Output ripple voltage	<30 mV @ CCM
Output current rating	6A
Operating frequency	500 kHz

8.2.2 Detailed Design Procedure

8.2.2.1 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the V_{FB} pin. TI recommends to use 1% tolerance or better divider resistors. Start by using Equation 5 to calculate V_{OUT}. R_5 is optional and can be used to measure the control loop's frequency response.

To improve efficiency at very light loads consider using larger value resistors. If the resistance is too high the device will be more susceptible to noise and voltage errors from the V_{FB} input current will be more noticeable. Please note that dynamically adjusting output voltage is not recommended.

$$V_{OUT} = 0.6 \times \left(1 + \frac{R6}{R7}\right) \quad (5)$$

8.2.2.2 Output Filter Selection

The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (6)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP3 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of Equation 6 is located below the high frequency zero but close enough that the phase boost provided be the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 4.

Table 4. Recommended Component Values

OUTPUT VOLTAGE(1) (V)	R6(2) (kΩ)	R7 (kΩ)	L1 (µH)	C_{OUT}(3) (µF)			C9 (pF)(4)	R8 (kΩ)(4)
				MIN	TYP	MAX		
1.05	7.5	10.0	1	30	35	100		
1.2	10	10.0	1	30	35	100		
1.8	20	10.0	1.2	30	35	100		
3.3	45.3	10.0	2.2	20	35	100	100 to 220	20
5	73.2	10.0	3.3	20	30	100	100 to 220	20
12	191	10.0	5.6	25	30	100	100 to 220	20

(1) Please use the recommended L1 and C_{OUT} combination of the higher and closest output rail for unlisted output rails.
(2) R6=0Ω for V_{OUT}=0.6V
(3) C_{OUT} is the sum of effective output capacitance. In this datasheet the effective capacitance is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of effective capacitance is provided. Refer to the information of DC bias and temperature characteristics from manufacturers of ceramic capacitors.
(4) R8 and C9 can be used to improve the load transient response or improve the loop-phase margin. The application report Optimizing Transient Response of Internally Compensated DCDC Converters with Feed-forward Capacitor is helpful when experimenting with a feed-forward capacitor.

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using Equation 7, Equation 8, and Equation 9. The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current.

Use 500 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of Equation 8 and the RMS current of Equation 9.

$$Il_{P-P} = \frac{V_{OUT}}{V_{IN(MAX)}} \cdot \frac{V_{IN(MAX)} - V_{OUT}}{L_O \cdot f_{SW}} \tag{7}$$

$$Il_{PEAK} = I_O + \frac{Il_{P-P}}{2} \tag{8}$$

$$I_{LO(RMS)} = \sqrt{I_O{}^2 + \frac{1}{12} Il_{P-P}{}^2} \tag{9}$$

For this design example, the calculated peak current is 7.28A and the calculated RMS current is 6.05 A. The inductor used is IHLP3232DZER3R3M11 with a peak current rating of 10.5A and an RMS current rating of 9.7A.

The capacitor value and ESR determines the amount of output voltage ripple. TheTPS56637 is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20 µF to 100 µF. Use Equation 10 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_O \cdot f_{SW}} \tag{10}$$

For this design two MuRata GRM32ER71E226KE15L 22-µF output capacitors are used so that the effective capacitance is 31.08 µF at DC biased voltage of 5V. The calculated RMS current is 0.738A and each output capacitor is rated for 4 A.

8.2.2.3 Input Capacitor Selection

The TPS56637 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN to PGND pin is recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage. The input voltage ripple can be calculated using Equation 11.

$$\Delta V_{in} = \frac{I_{outmax} \cdot 0.25}{C_{in} \cdot f_{SW}} \tag{11}$$

The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by Equation 12:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \tag{12}$$

8.2.2.4 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor(C4) must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

8.2.3 Application Curves

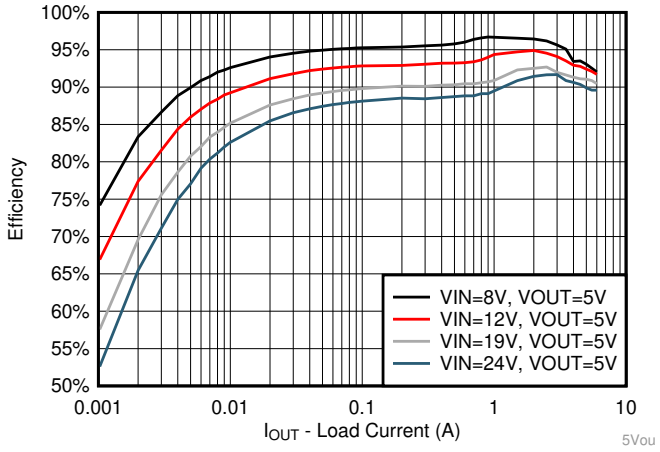


Figure 18. Efficiency

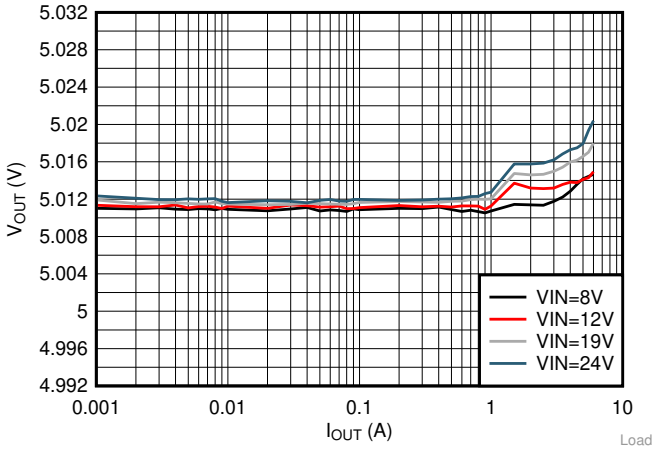


Figure 19. Load Regulation

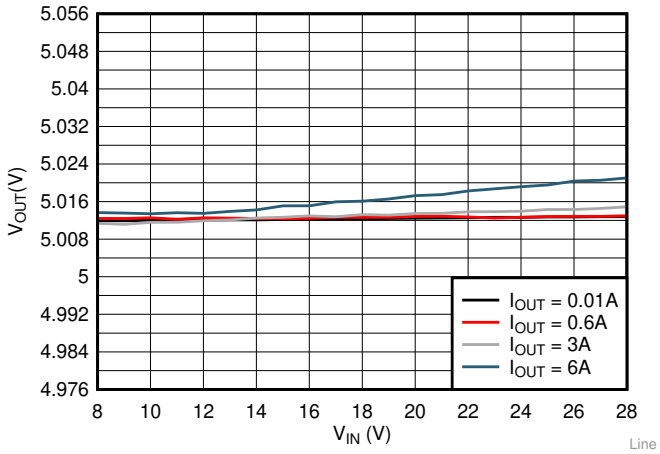


Figure 20. Line Regulation

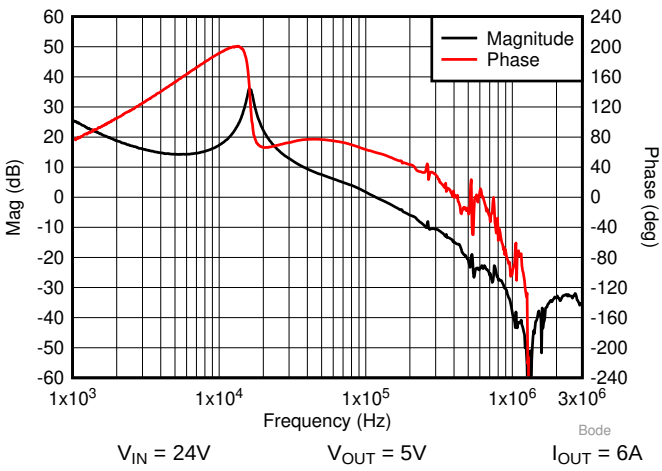


Figure 21. Bode Plot

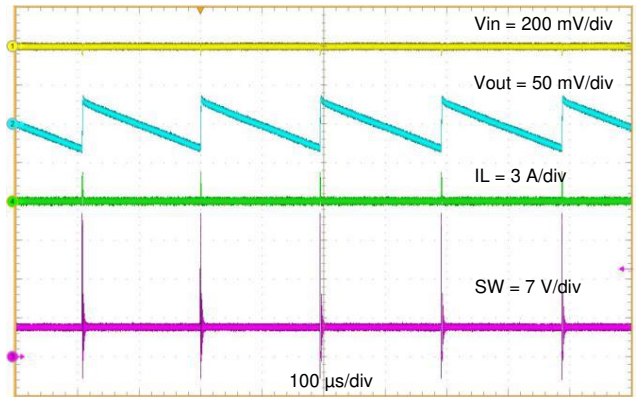


Figure 22. Steady State Waveforms, I_{OUT} = 0.01 A

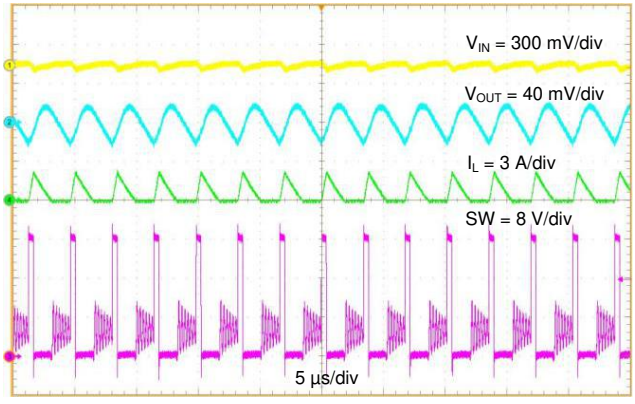


Figure 23. Steady State Waveforms, I_{OUT}= 0.6 A

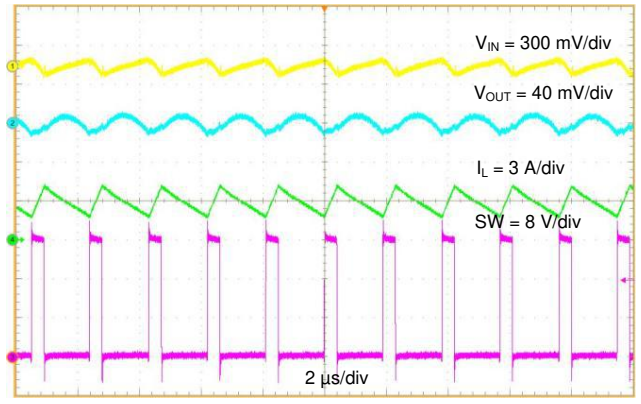


Figure 24. Steady State Waveforms, I_{OUT}= 3 A

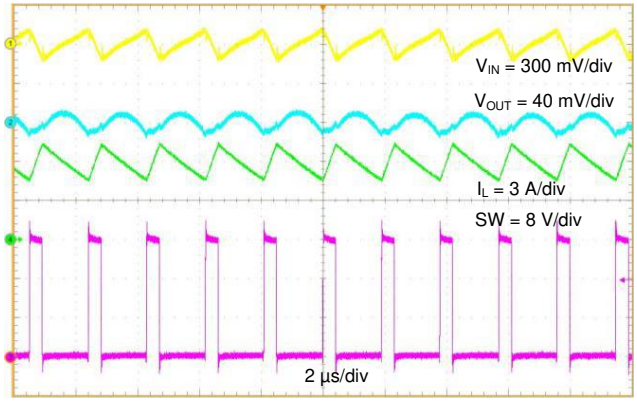


Figure 25. Steady State Waveforms, I_{OUT}= 6 A

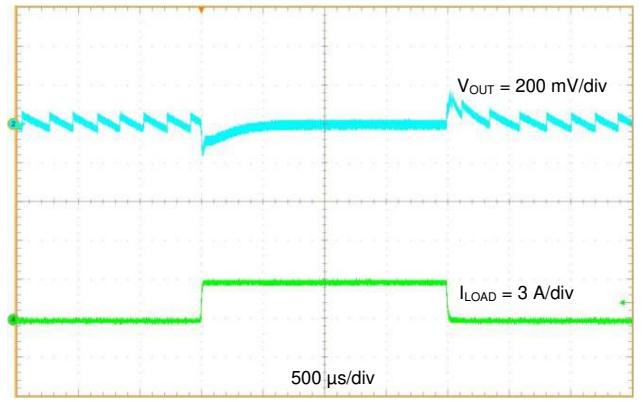


Figure 26. Transient Response 0 to 3 A

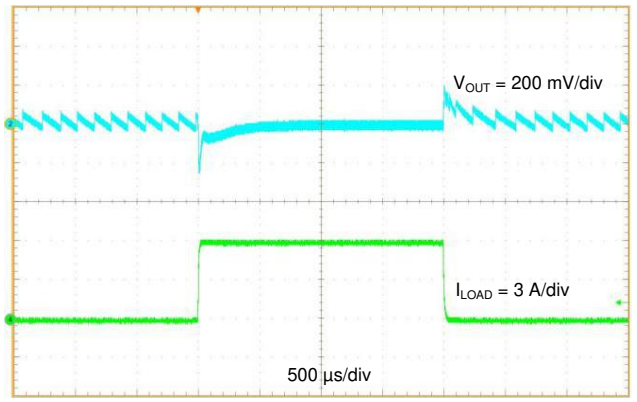


Figure 27. Transient Response 0 to 6 A

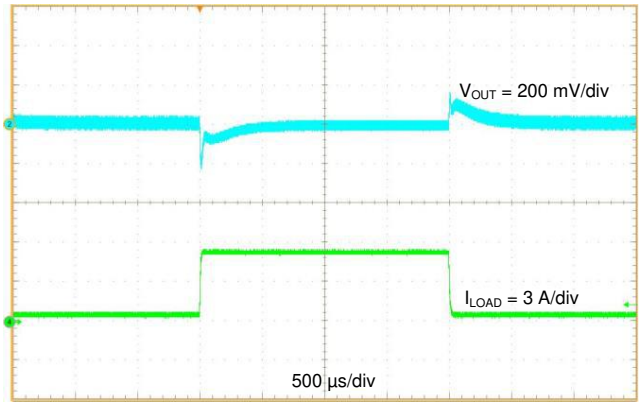


Figure 28. Transient Response 0.6 to 5.4 A

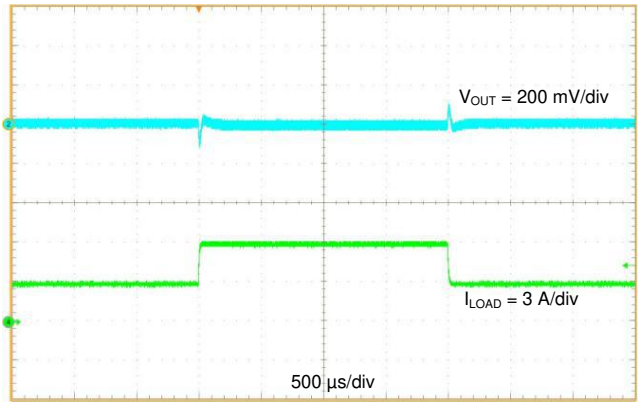


Figure 29. Transient Response 3 to 6 A

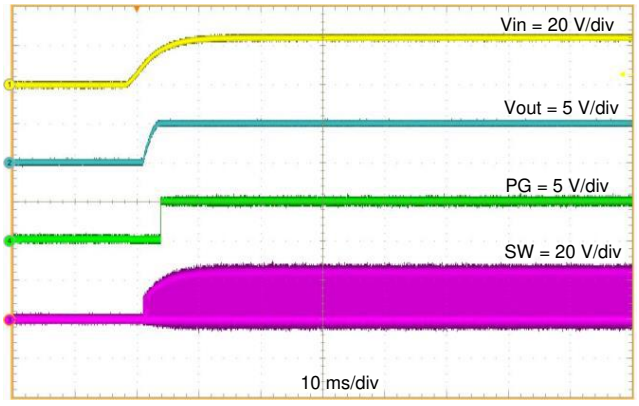


Figure 30. Startup Relative to V_{IN}

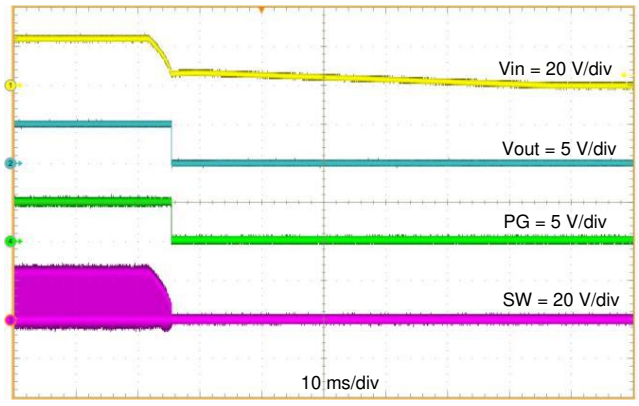


Figure 31. Shutdown Relative to V_{IN}

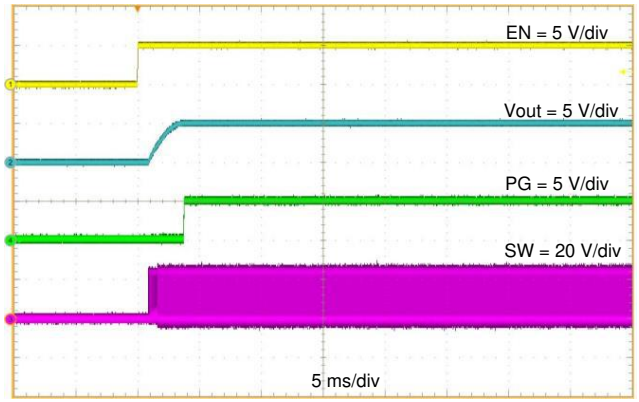


Figure 32. Enable Relative to EN

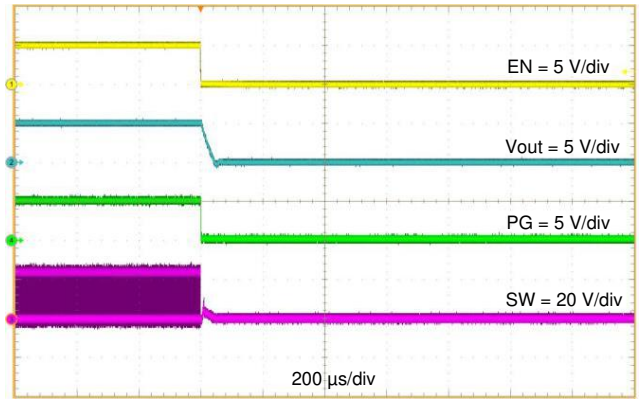


Figure 33. Disable Relative to EN

9 Power Supply Recommendations

The TPS56637 is designed to operate from input supply voltage in the range of 4.5 V to 28 V. Buck converters require the input voltage to be higher than the output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS56637 circuit, some additional input bulk capacitance is recommended.

10 Layout

10.1 Layout Guidelines

1. Recommend a four-layer PCB for good thermal performance and with maximum ground plane.
2. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
3. Putting at least two vias for VIN and GND traces, and as close as possible to the pins.
4. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
5. Provide sufficient vias for the input capacitor and output capacitor.
6. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
7. Do not allow switching current to flow under the device.
8. A separate VOUT path should be connected to the upper feedback resistor.
9. Make a Kelvin connection to the GND pin for the feedback path.
10. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
11. The trace of the VFB node should be as small as possible to avoid noise coupling.
12. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

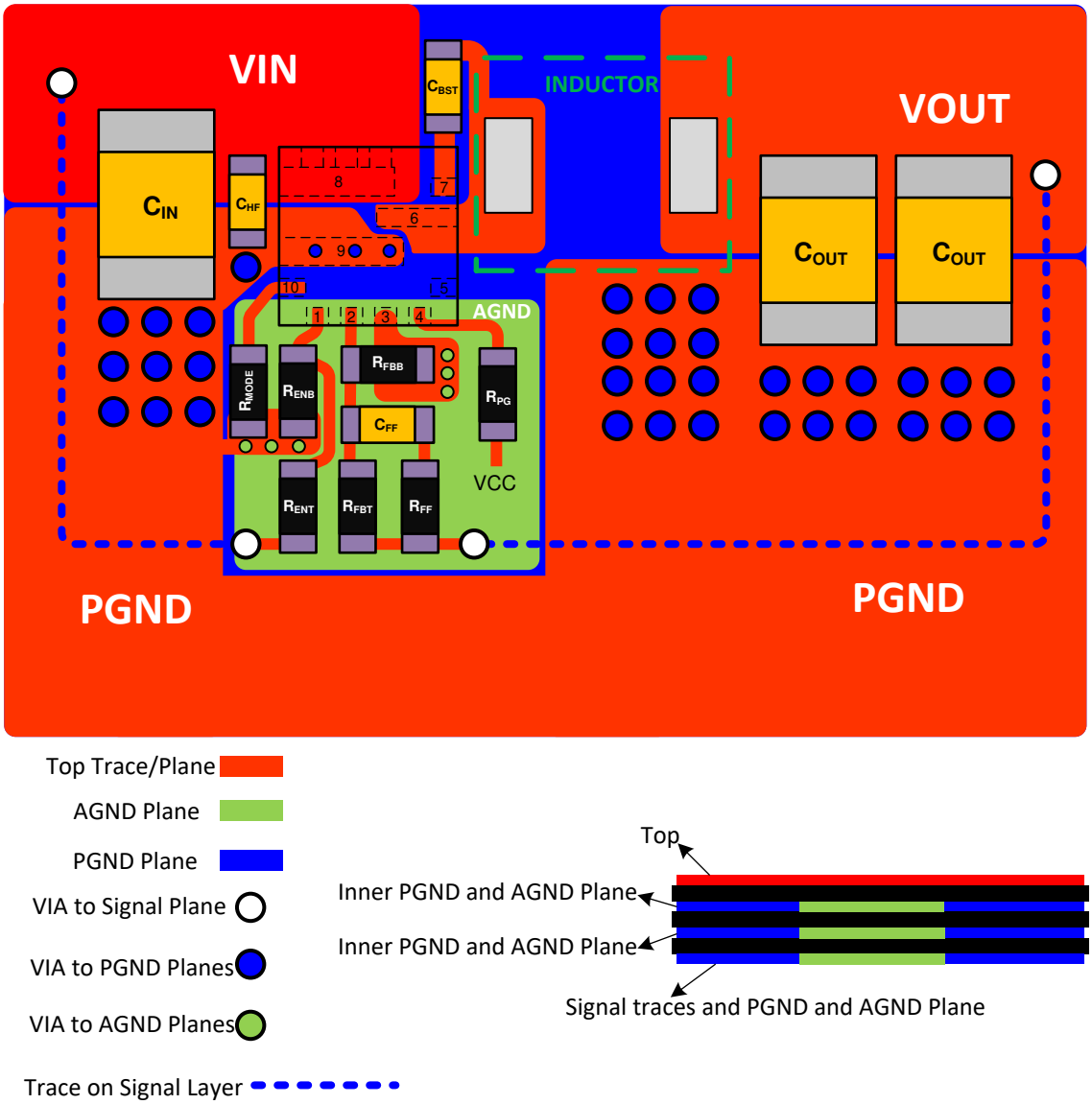


Figure 34. TPS56637 Layout

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following: Texas Instruments, *TPS56637EVM-029 6-A, Regulator Evaluation Module* user's guide

- Texas Instruments, *TPS56637EVM-029 6-A, Regulator Evaluation Module* user's guide
-

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

D-CAP3, Eco-mode, HotRod, DCAP3, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS56637RPAR	ACTIVE	VQFN-HR	RPA	10	3000	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 150	T56637	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

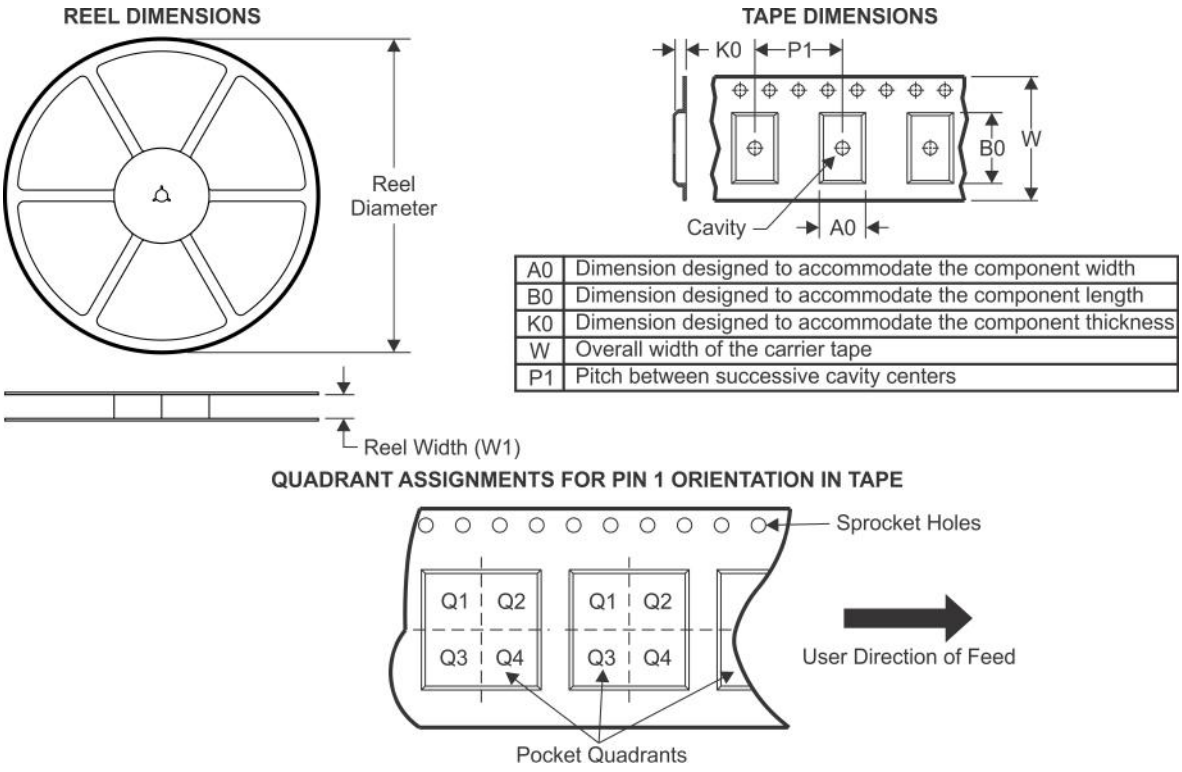
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

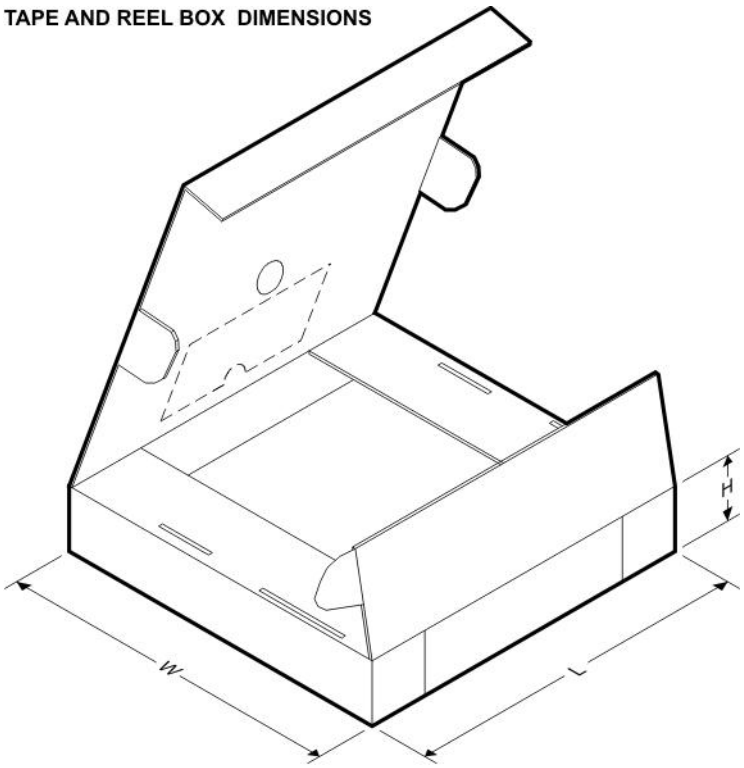


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS56637RPAR	VQFN-HR	RPA	10	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

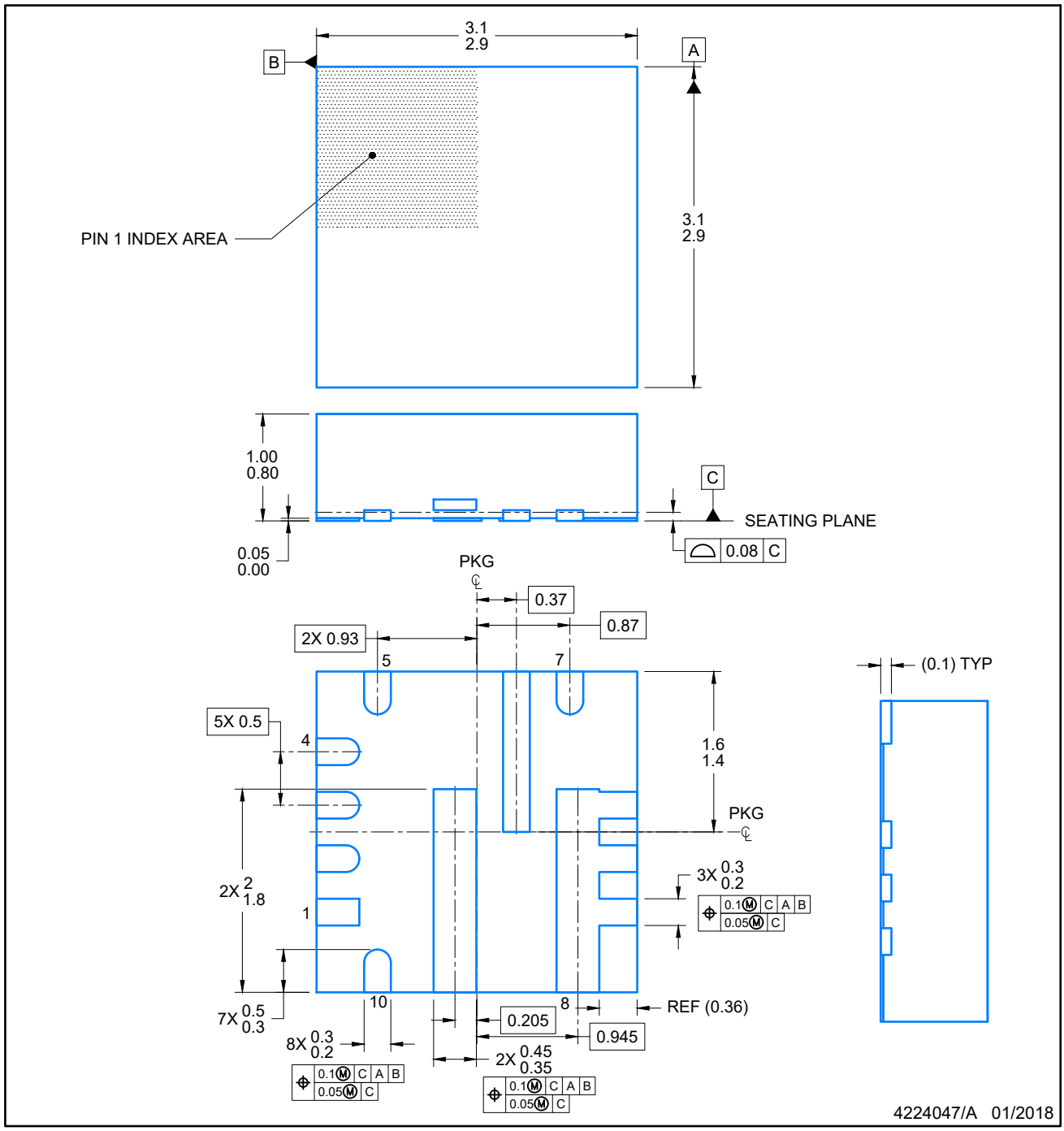
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS56637RPAR	VQFN-HR	RPA	10	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RPA0010A

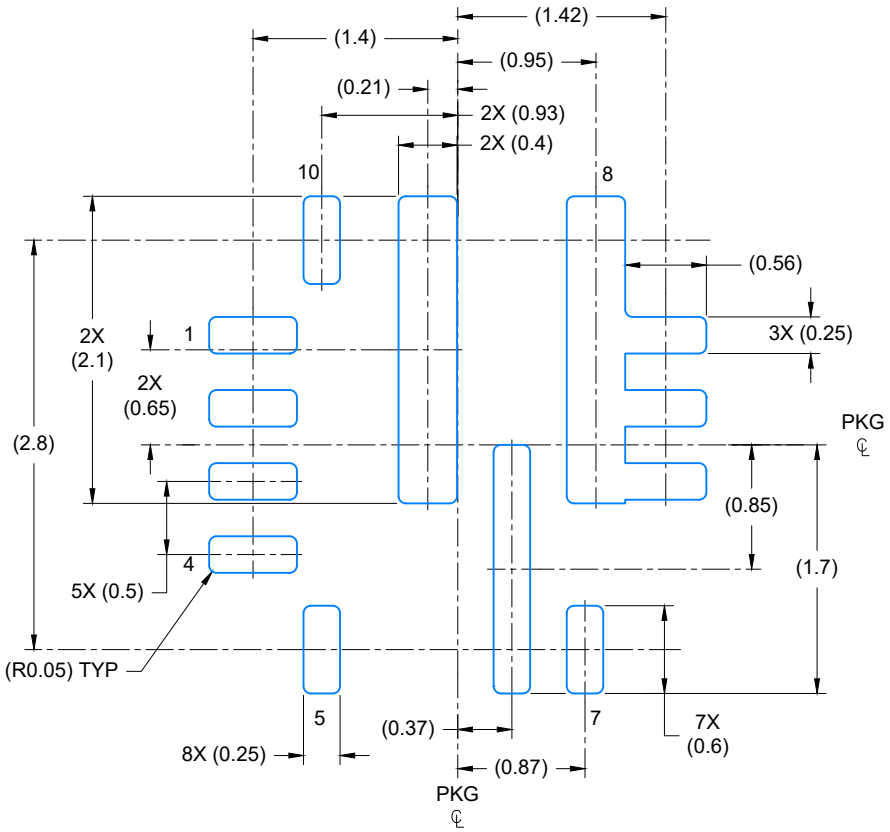
VQFN-HR - 1 mm max height

PLASTIC QUAD FLAT-NO LEAD

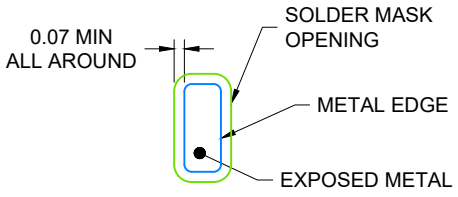


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON SOLDER MASK
DEFINED

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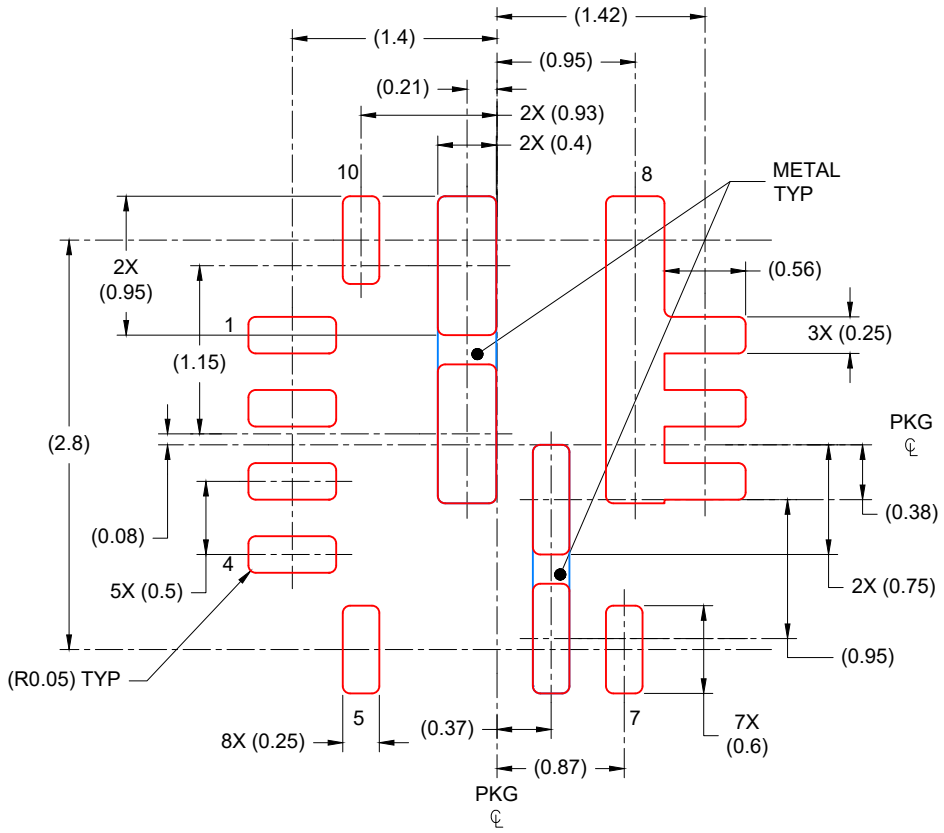
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
PADS 6 and 9: 89% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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